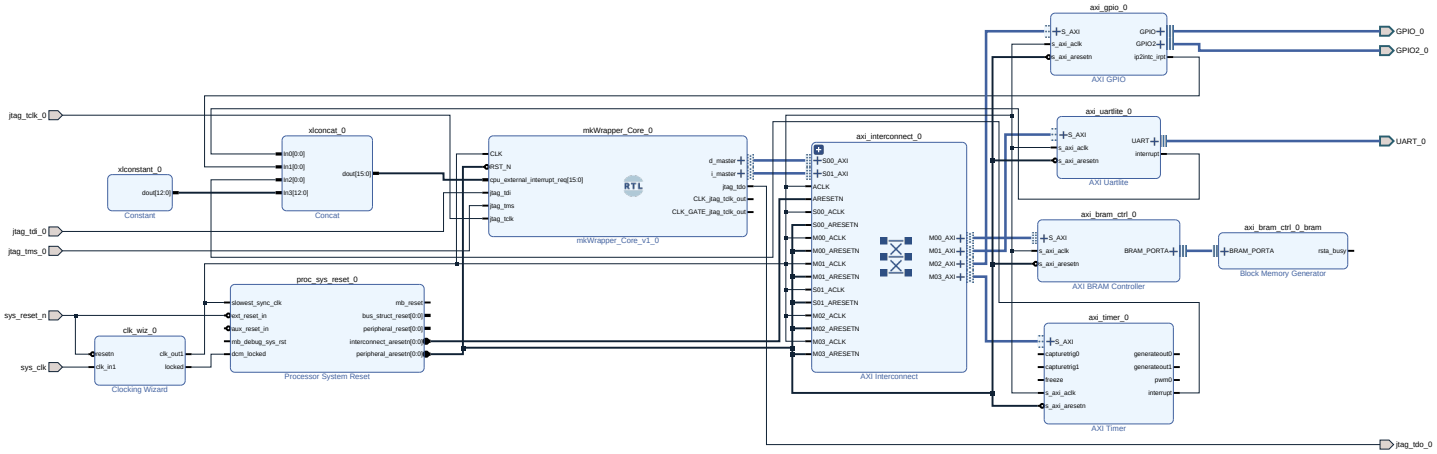
axi_gpio_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
GPIO2
ip2intc_irpt
AXI GPIO
GPIO_0
GPIO2_0
axi_uartlite_0
S_AXI
s_axi_aclk
s_axi_aresetn
UART
interrupt
AXI Uartlite
UART_0
axi_bram_ctrl_0
S_AXI
s_axi_aclk
s_axi_aresetn
BRAM_PORTA
AXI BRAM Controller
axi_bram_ctrl_0_bram
BRAM_PORTA
rsta_busy
Block Memory Generator
axi_timer_0
S_AXI
capturetrig0
capturetrig1
freeze
s_axi_aclk
s_axi_aresetn
generateout0
generateout1
pwm0
interrupt
AXI Timer
jtag_tclk_0
xlconcat_0
In0[0:0]
In1[0:0]
In2[0:0]
In3[12:0]
dout[15:0]
Concat
xlconstant_0
dout[12:0]
Constant
mkWrapper_Core_0
CLK
RST_N
cpu_external_interrupt_req[15:0]
jtag_tdi
jtag_tms
jtag_tclk
d_master
i_master
jtag_tdo
CLK_jtag_tclk_out
CLK_GATE_jtag_tclk_out
RTL
mkWrapper_Core_v1_0
axi_interconnect_0
S00_AXI
S01_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
S01_ACLK
S01_ARESETN
M02_ACLK
M02_ARESETN
M03_ACLK
M03_ARESETN
M00_AXI
M01_AXI
M02_AXI
M03_AXI
AXI Interconnect
jtag_tdi_0
jtag_tms_0
proc_sys_reset_0
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
sys_reset_n
clk_wiz_0
resetn
clk_in1
clk_out1
locked
Clocking Wizard
sys_clk
jtag_tdo_0