

GMCLIB User's Guide

ARM[®] Cortex[®] M0+



Contents

Chapter 1 Library	5
1.1 Introduction.....	5
1.1.1 Overview.....	5
1.1.2 Data types.....	5
1.1.3 API definition.....	5
1.1.4 Supported compilers.....	6
1.1.5 Library configuration.....	6
1.1.6 Special issues.....	6
1.2 Library integration into project (MCUXpresso IDE)	6
1.3 Library integration into project (Keil µVision)	9
1.4 Library integration into project (IAR Embedded Workbench)	17
Chapter 2 Algorithms in detail	23
2.1 GMCLIB_Clark.....	23
2.1.1 Available versions.....	23
2.1.2 Declaration.....	23
2.1.3 Function use.....	23
2.2 GMCLIB_ClarkInv.....	24
2.2.1 Available versions.....	24
2.2.2 Declaration.....	24
2.2.3 Function use.....	24
2.3 GMCLIB_Park.....	25
2.3.1 Available versions.....	25
2.3.2 Declaration.....	25
2.3.3 Function use.....	26
2.4 GMCLIB_ParkInv.....	26
2.4.1 Available versions.....	26
2.4.2 Declaration.....	27
2.4.3 Function use.....	27
2.5 GMCLIB_DecouplingPMSM.....	28
2.5.1 Available versions.....	29
2.5.2 GMCLIB_DECOUPLINGPMSM_T_A32 type description.....	30
2.5.3 Declaration.....	30
2.5.4 Function use.....	30
2.6 GMCLIB_DTCompLut1D.....	31
2.6.1 Available versions.....	33
2.6.2 GMCLIB_DTCOMPLUT1D_T_F16 type description.....	34
2.6.3 Declaration.....	34
2.6.4 Function use.....	34
2.7 GMCLIB_ElimDcBusRipFOC.....	35
2.7.1 Available versions.....	37
2.7.2 Declaration.....	38
2.7.3 Function use.....	38
2.8 GMCLIB_ElimDcBusRip.....	38
2.8.1 Available versions.....	41
2.8.2 Declaration.....	41
2.8.3 Function use.....	41
2.9 GMCLIB_SvmStdShifted.....	42
2.9.1 Available versions.....	45
2.9.1.1 GMCLIB_SVMSTDSHIFTED_T_F16 type description.....	46

2.9.2 GMCLIB_ADC_CONFIG_T_F16 type description.....	46
2.9.3 GMCLIB_PWM_CONFIG_T_F16 type description.....	46
2.9.4 GMCLIB_PHASE_INDEX_T type description.....	47
2.9.5 Declaration.....	47
2.9.6 Function use.....	47
2.10 GMCLIB_SvmStd.....	48
2.10.1 Available versions.....	59
2.10.2 Declaration.....	59
2.10.3 Function use.....	60
2.11 GMCLIB_SvmIct.....	60
2.11.1 Available versions.....	62
2.11.2 Declaration.....	62
2.11.3 Function use.....	62
2.12 GMCLIB_SvmU0n.....	63
2.12.1 Available versions.....	64
2.12.2 Declaration.....	65
2.12.3 Function use.....	65
2.13 GMCLIB_SvmU7n.....	65
2.13.1 Available versions.....	67
2.13.2 Declaration.....	67
2.13.3 Function use.....	68
2.14 GMCLIB_SvmDpwm.....	68
2.14.1 Available versions.....	69
2.14.2 Declaration.....	70
2.14.3 Function use.....	70
2.15 GMCLIB_SvmExDpwm.....	70
2.15.1 Available versions.....	72
2.15.2 Declaration.....	72
2.15.3 Function use.....	72
Appendix A Library types.....	74
A.1 bool_t.....	74
A.2 uint8_t.....	74
A.3 uint16_t.....	75
A.4 uint32_t.....	76
A.5 int8_t.....	76
A.6 int16_t.....	77
A.7 int32_t.....	77
A.8 frac8_t.....	78
A.9 frac16_t.....	79
A.10 frac32_t.....	79
A.11 acc16_t.....	80
A.12 acc32_t.....	81
A.13 float_t.....	81
A.14 GMCLIB_3COOR_T_F16.....	84
A.15 GMCLIB_3COOR_T_FLT.....	84
A.16 GMCLIB_2COOR_AB_T_F16.....	85
A.17 GMCLIB_2COOR_AB_T_F32.....	85
A.18 GMCLIB_2COOR_ALBE_T_F16.....	86
A.19 GMCLIB_2COOR_ALBE_T_FLT.....	86
A.20 GMCLIB_2COOR_DQ_T_F16.....	86
A.21 GMCLIB_2COOR_DQ_T_F32.....	87

A.22 GMCLIB_2COOR_DQ_T_FLT.....	87
A.23 GMCLIB_2COOR_SINCOS_T_F16.....	87
A.24 GMCLIB_2COOR_SINCOS_T_FLT.....	88
A.25 FALSE.....	88
A.26 TRUE.....	89
A.27 FRAC8.....	89
A.28 FRAC16.....	89
A.29 FRAC32.....	90
A.30 ACC16.....	90
A.31 ACC32.....	90

Chapter 1

Library

1.1 Introduction

1.1.1 Overview

This user's guide describes the General Motor Control Library (GMCLIB) for the family of ARM Cortex M0+ core-based microcontrollers. This library contains optimized functions.

1.1.2 Data types

GMCLIB supports several data types: (un)signed integer, fractional, and accumulator. The integer data types are useful for general-purpose computation; they are familiar to the MPU and MCU programmers. The fractional data types enable powerful numeric and digital-signal-processing algorithms to be implemented. The accumulator data type is a combination of both; that means it has the integer and fractional portions.

The following list shows the integer types defined in the libraries:

- **Unsigned 16-bit integer**— $\langle 0 ; 65535 \rangle$ with the minimum resolution of 1
- **Signed 16-bit integer**— $\langle -32768 ; 32767 \rangle$ with the minimum resolution of 1
- **Unsigned 32-bit integer**— $\langle 0 ; 4294967295 \rangle$ with the minimum resolution of 1
- **Signed 32-bit integer**— $\langle -2147483648 ; 2147483647 \rangle$ with the minimum resolution of 1

The following list shows the fractional types defined in the libraries:

- **Fixed-point 16-bit fractional**— $\langle -1 ; 1 - 2^{-15} \rangle$ with the minimum resolution of 2^{-15}
- **Fixed-point 32-bit fractional**— $\langle -1 ; 1 - 2^{-31} \rangle$ with the minimum resolution of 2^{-31}

The following list shows the accumulator types defined in the libraries:

- **Fixed-point 16-bit accumulator**— $\langle -256.0 ; 256.0 - 2^{-7} \rangle$ with the minimum resolution of 2^{-7}
- **Fixed-point 32-bit accumulator**— $\langle -65536.0 ; 65536.0 - 2^{-15} \rangle$ with the minimum resolution of 2^{-15}

1.1.3 API definition

GMCLIB uses the types mentioned in the previous section. To enable simple usage of the algorithms, their names use set prefixes and postfixes to distinguish the functions' versions. See the following example:

```
f32Result = MLIB_Mac_F32lss(f32Accum, f16Mult1, f16Mult2);
```

where the function is compiled from four parts:

- **MLIB**—this is the library prefix
- **Mac**—the function name—Multiply-Accumulate
- **F32**—the function output type
- **lss**—the types of the function inputs; if all the inputs have the same type as the output, the inputs are not marked

The input and output types are described in the following table:

Table 1. Input/output types

Type	Output	Input
frac16_t	F16	s
frac32_t	F32	l
acc32_t	A32	a

1.1.4 Supported compilers

GMCLIB for the ARM Cortex M0+ core is written in C language or assembly language with C-callable interface depending on the specific function. The library is built and tested using the following compilers:

- MCUXpresso IDE
- IAR Embedded Workbench
- Keil μ Vision

For the MCUXpresso IDE, the library is delivered in the *gmclib.a* file.

For the Kinetis Design Studio, the library is delivered in the *gmclib.a* file.

For the IAR Embedded Workbench, the library is delivered in the *gmclib.a* file.

For the Keil μ Vision, the library is delivered in the *gmclib.lib* file.

The interfaces to the algorithms included in this library are combined into a single public interface include file, *gmclib.h*. This is done to lower the number of files required to be included in your application.

1.1.5 Library configuration

GMCLIB for the ARM Cortex M0+ core is written in C language or assembly language with C-callable interface depending on the specific function. Some functions from this library are inline type, which are compiled together with project using this library. The optimization level for inline function is usually defined by the specific compiler setting. It can cause an issue especially when high optimization level is set. Therefore the optimization level for all inline assembly written functions is defined by compiler pragmas using macros. The configuration header file *RTCESL_cfg.h* is located in: *specific library folder\MLIB\Include*. The optimization level can be changed by modifying the macro value for specific compiler. In case of any change the library functionality is not guaranteed.

Similarly as optimization level the Memory-mapped divide and square root module support can be disable or enable by defined symbol *RTCESL_MMDVSQ_ON* or *RTCESL_MMDVSQ_OFF* in project setting described in the Memory-mapped divide and square root support chapter for specific compiler.

1.1.6 Special issues

1. The equations describing the algorithms are symbolic. If there is positive 1, the number is the closest number to 1 that the resolution of the used fractional type allows. If there are maximum or minimum values mentioned, check the range allowed by the type of the particular function version.
2. The library functions that round the result (the API contains *Rnd*) round to nearest (half up).

1.2 Library integration into project (MCUXpresso IDE)

This section provides a step-by-step guide on how to quickly and easily include GMCLIB into any MCUXpresso SDK example or new SDK project using MCUXpresso IDE. The SDK based project uses RTCESL from SDK package.

Adding RTCESL component to project

The MCUXpresso SDK package is necessary to add any example or new project and RTCESL component. In case the package has not been downloaded go to mcuxpresso.nxp.com, build the final MCUXpresso SDK package for required board and download it.

After package is downloaded, open the MCUXpresso IDE and drag&drop the SDK package in zip format to the Installed SDK window of the MCUXpresso IDE. After SDK package is dropped the message accepting window appears as can be show in following figure.

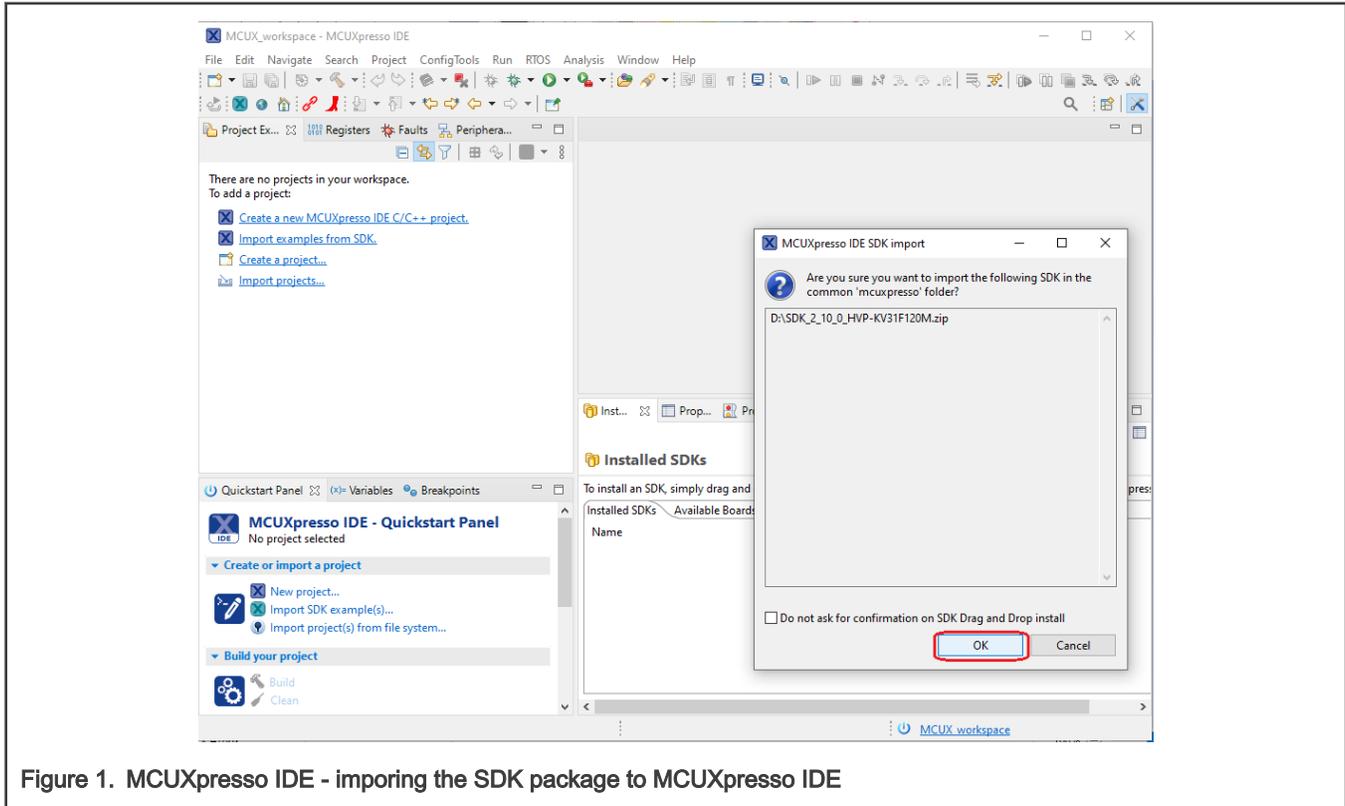


Figure 1. MCUXpresso IDE - importing the SDK package to MCUXpresso IDE

Click OK to confirm the SDK package import. Find the Quickstart panel in left bottom part of the MCUXpresso IDE and click New project... item or Import SDK example(s)... to add rtcesl component to the project.

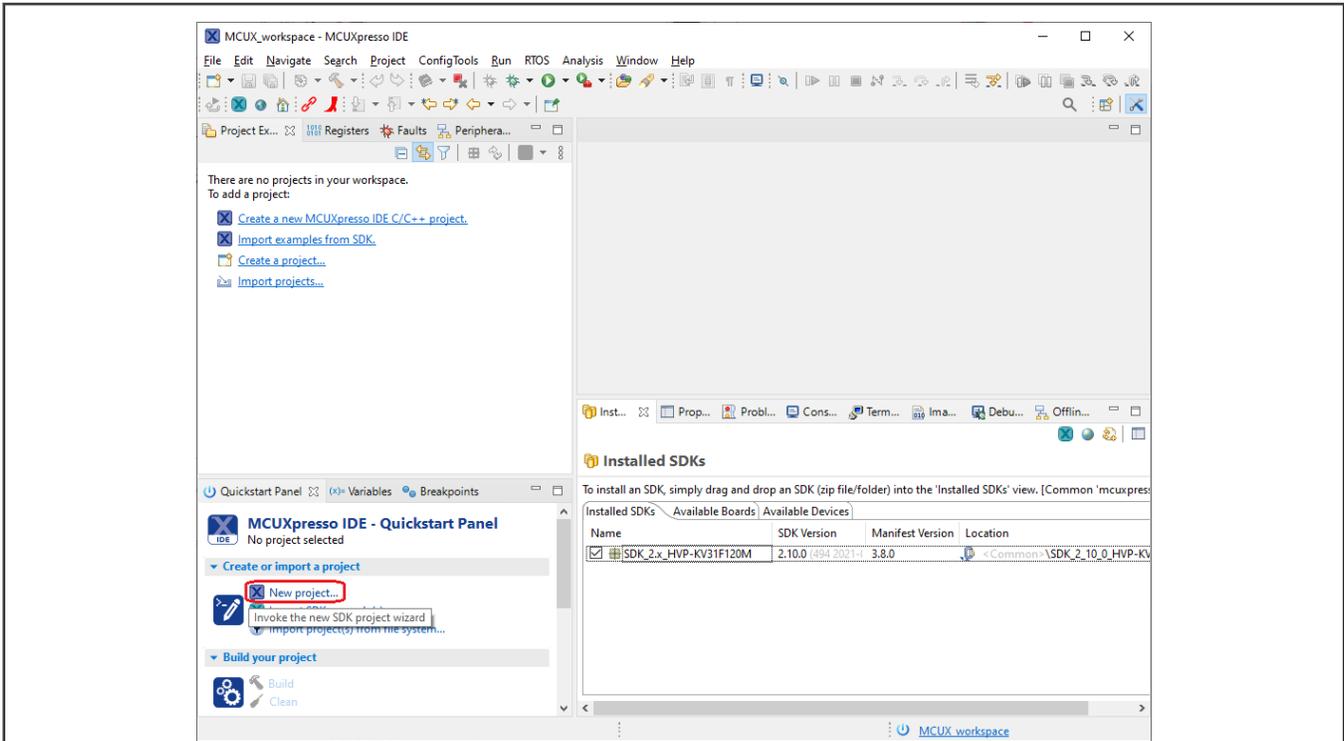


Figure 2. MCUXpresso IDE - create new project or Import SDK example(s)

Then select your board, and click Next button.

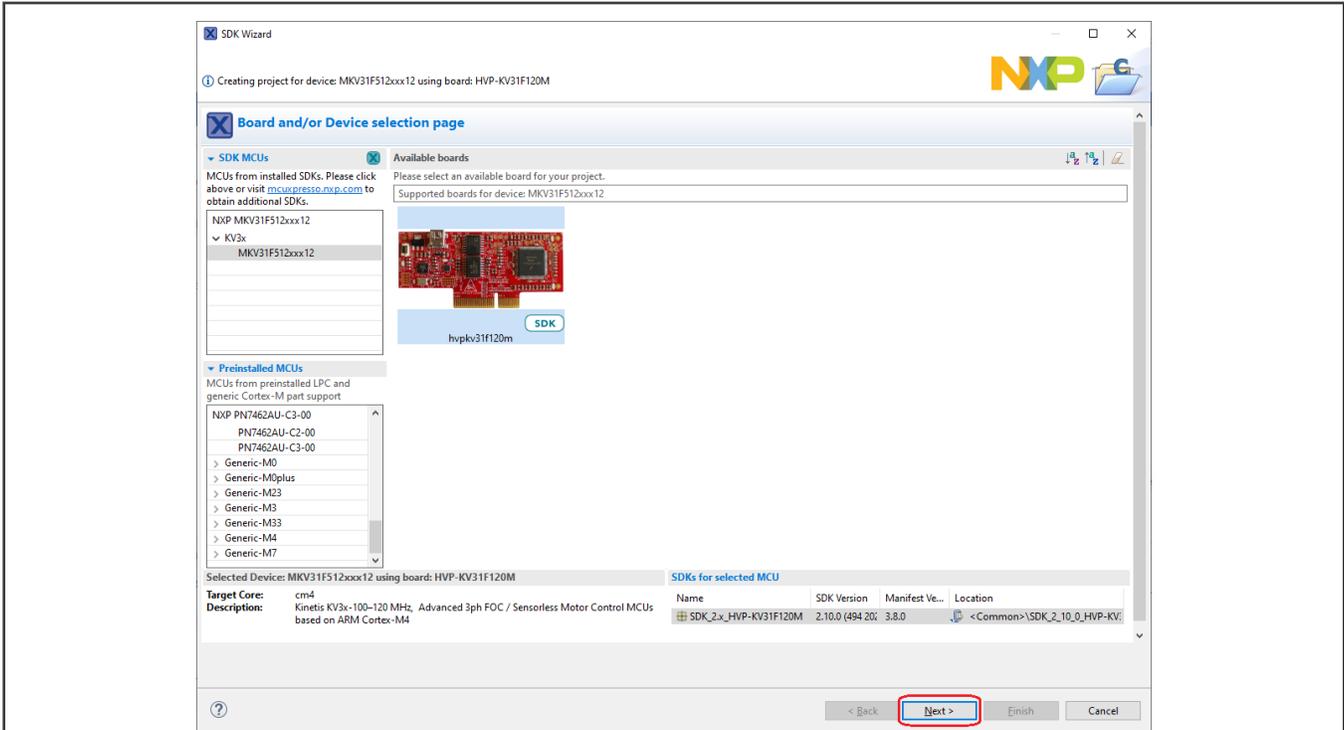


Figure 3. MCUXpresso IDE - selecting the board

Find the Middleware tab in the Components part of the window and click on the checkbox to be the rtcesl component ticked. Last step is to click the Finish button and wait for project creating with all RTCESL libraries and include paths.

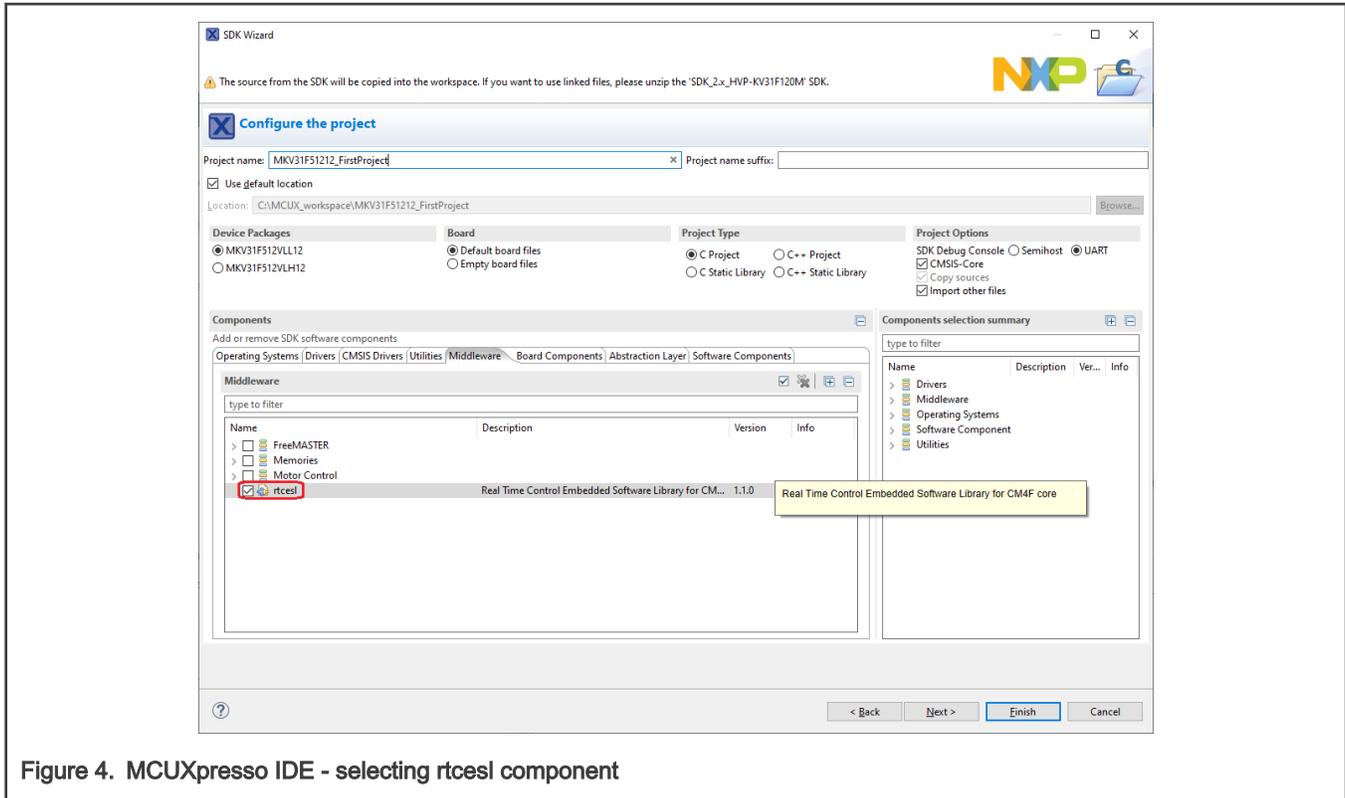


Figure 4. MCUXpresso IDE - selecting rtcesl component

Type the `#include` syntax into the code where you want to call the library functions. In the left-hand dialog, open the required .c file. After the file opens, include the following lines into the `#include` section:

```
#include "mlib.h"
#include "gflib.h"
#include "gmclib.h"
```

When you click the Build icon (hammer), the project is compiled without errors.

1.3 Library integration into project (Keil μ Vision)

This section provides a step-by-step guide on how to quickly and easily include GMCLIB into an empty project or any MCUXpresso SDK example or demo application projects using Keil μ Vision. This example uses the default installation path (C:\NXP\RTCESL\CM0_RTCESL_4.7_KEIL). If you have a different installation path, use that path instead. If any MCUXpresso SDK project is intended to use (for example hello_world project) go to [Memory-mapped divide and square root support](#) chapter otherwise read next chapter.

NXP pack installation for new project (without MCUXpresso SDK)

This example uses the NXP MKV10Z32xxx7 part, and the default installation path (C:\NXP\RTCESL\CM0_RTCESL_4.7_KEIL) is supposed. If the compiler has never been used to create any NXP MCU-based projects before, check whether the NXP MCU pack for the particular device is installed. Follow these steps:

1. Launch Keil μ Vision.
2. In the main menu, go to Project > Manage > Pack Installer....
3. In the left-hand dialog (under the Devices tab), expand the All Devices > Freescale (NXP) node.
4. Look for a line called "KVxx Series" and click it.
5. In the right-hand dialog (under the Packs tab), expand the Device Specific node.

6. Look for a node called "Keil::Kinetis_KVxx_DFP." If there are the Install or Update options, click the button to install/update the package. See [Figure 5](#).
7. When installed, the button has the "Up to date" title. Now close the Pack Installer.

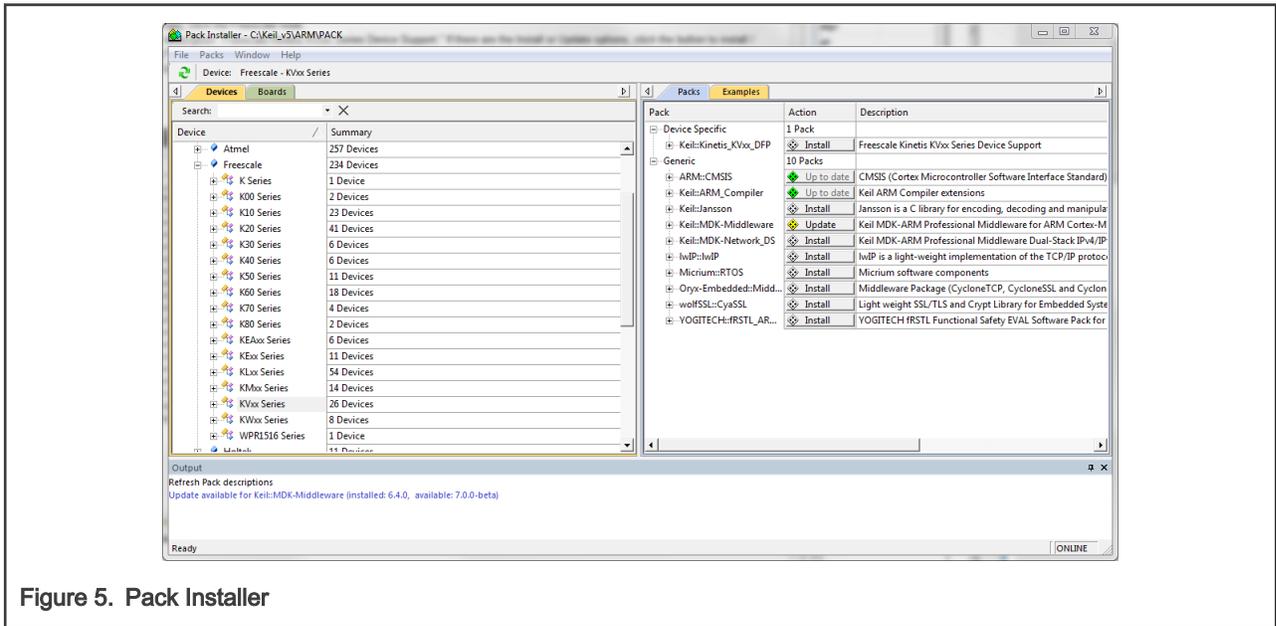


Figure 5. Pack Installer

New project (without MCUXpresso SDK)

To start working on an application, create a new project. If the project already exists and is opened, skip to the next section. Follow these steps to create a new project:

1. Launch Keil μ Vision.
2. In the main menu, select Project > New μ Vision Project..., and the Create New Project dialog appears.
3. Navigate to the folder where you want to create the project, for example C:\KeilProjects\MyProject01. Type the name of the project, for example MyProject01. Click Save. See [Figure 6](#).

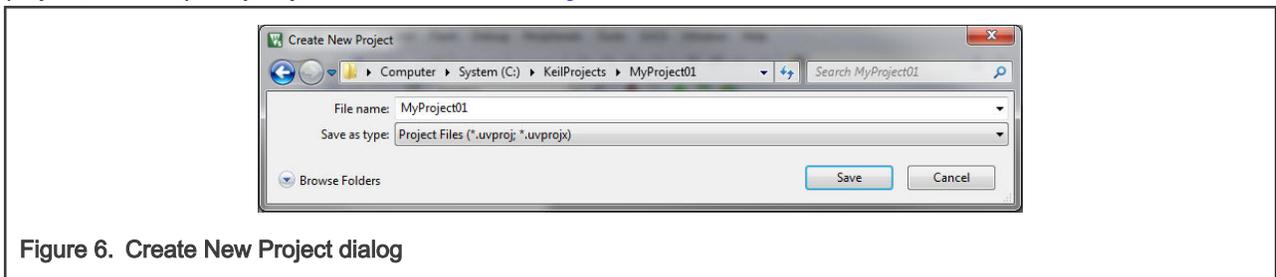


Figure 6. Create New Project dialog

4. In the next dialog, select the Software Packs in the very first box.
5. Type 'kv10' into the Search box, so that the device list is reduced to the KV10 devices.
6. Expand the KV10 node.
7. Click the MKV10Z32xxx7 node, and then click OK. See [Figure 7](#).

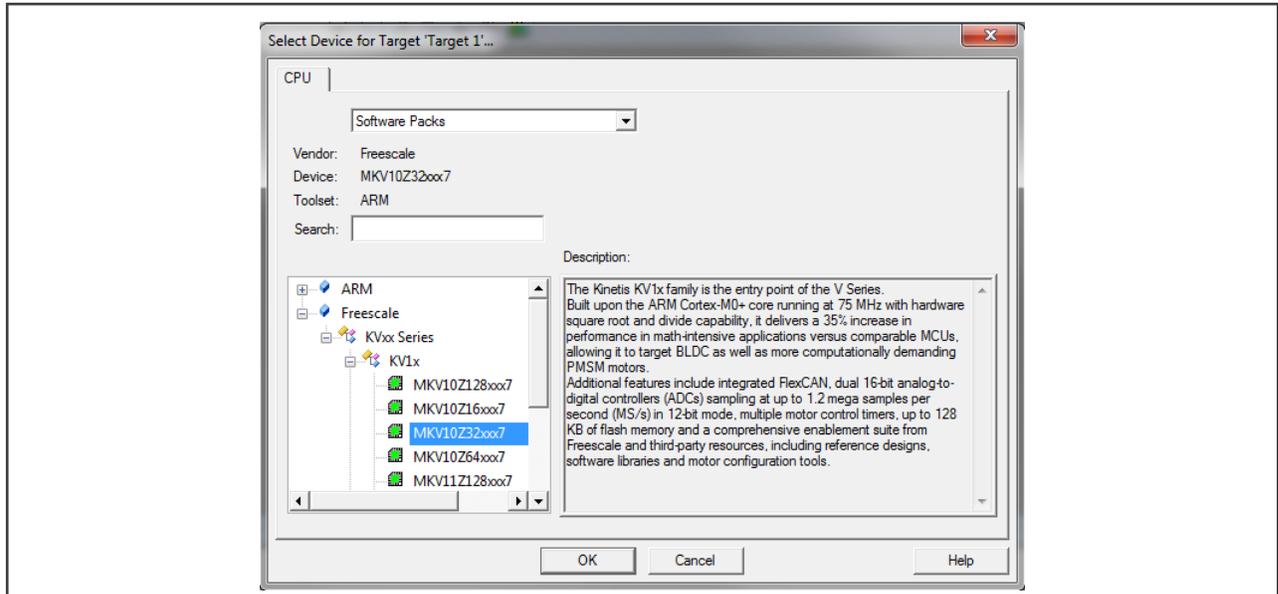


Figure 7. Select Device dialog

8. In the next dialog, expand the Device node, and tick the box next to the Startup node. See Figure 8.
9. Expand the CMSIS node, and tick the box next to the CORE node.

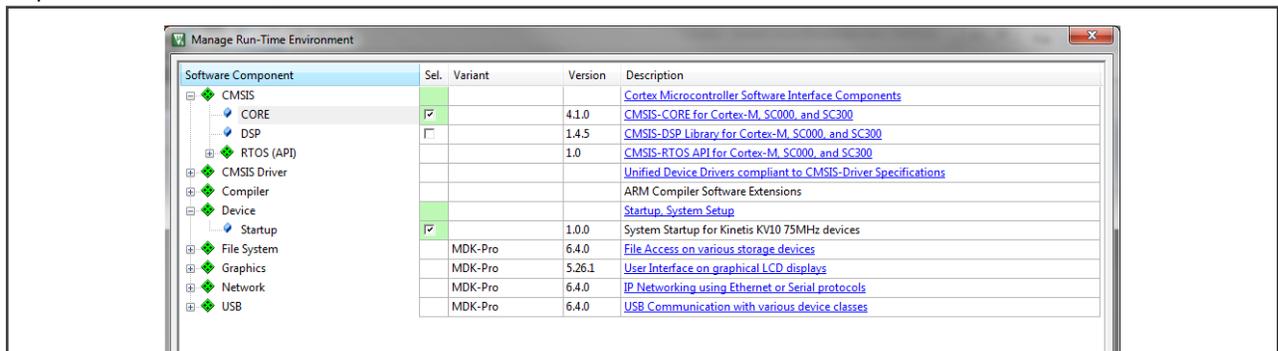


Figure 8. Manage Run-Time Environment dialog

10. Click OK, and a new project is created. The new project is now visible in the left-hand part of Keil µVision. See Figure 9.

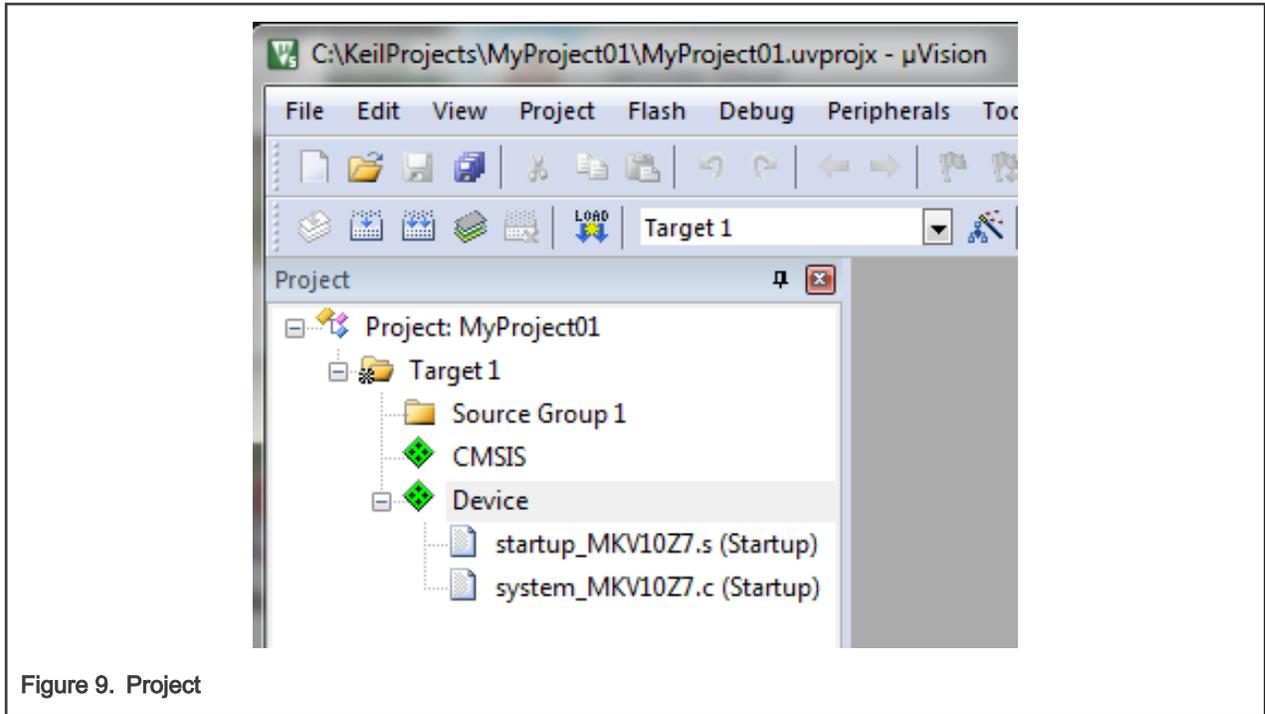


Figure 9. Project

Memory-mapped divide and square root support

Some Kinetis platforms contain a peripheral module dedicated for division and square root. This section shows how to turn the memory-mapped divide and square root (MMDV SQ) support on and off.

1. In the main menu, go to Project > Options for Target 'Target1'..., and a dialog appears.
2. Select the C/C++ tab. See [Figure 10](#).
3. In the Include Preprocessor Symbols text box, type the following:
 - RTCESL_MMDV SQ_ON—to turn the hardware division and square root support on
 - RTCESL_MMDV SQ_OFF—to turn the hardware division and square root support off

If neither of these two defines is defined, the hardware division and square root support is turned off by default.

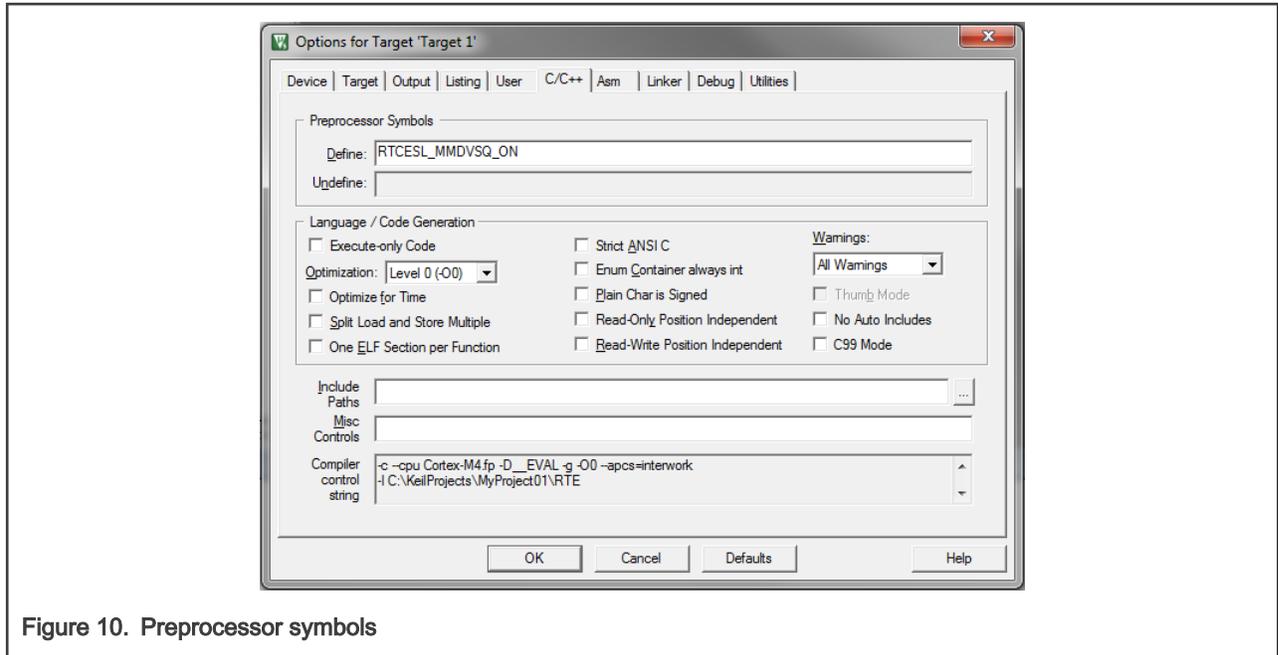


Figure 10. Preprocessor symbols

4. Click OK in the main dialog.

See the device reference manual to verify whether the device contains the MMDVDSQ module.

Linking the files into the project

GMCLIB requires MLIB and GFLIB to be included too. The following steps show how to include all dependent modules.

To include the library files in the project, create groups and add them.

1. Right-click the Target 1 node in the left-hand part of the Project tree, and select Add Group... from the menu. A new group with the name New Group is added.
2. Click the newly created group, and press F2 to rename it to RTCESL.
3. Right-click the RTCESL node, and select Add Existing Files to Group 'RTCESL'... from the menu.
4. Navigate into the library installation folder C:\NXP\RTCESL\CM0_RTCESEL_4.7_KEIL\MLIB\Include, and select the *mllib.h* file. If the file does not appear, set the Files of type filter to Text file. Click Add. See [Figure 11](#).

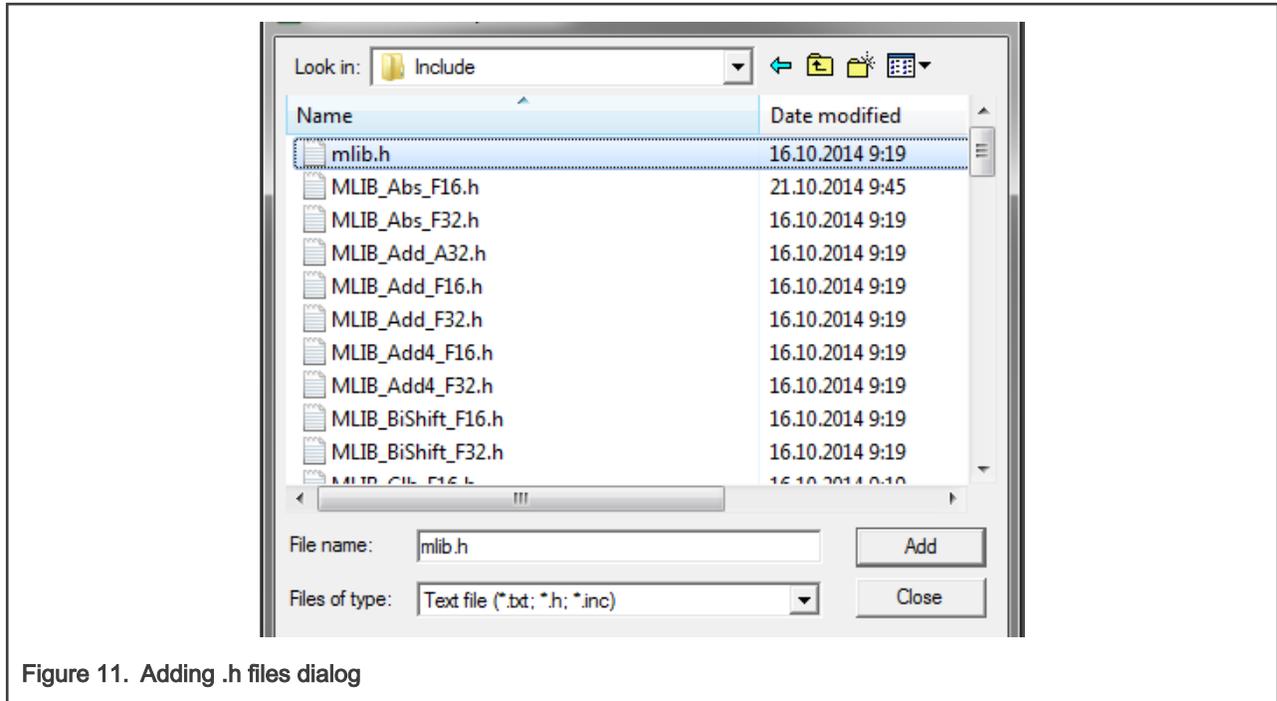


Figure 11. Adding .h files dialog

- Navigate to the parent folder C:\NXP\RTCESL\CM0_RTCESEL_4.7_KEIL\MLIB, and select the *mlib.lib* file. If the file does not appear, set the Files of type filter to Library file. Click Add. See Figure 12.

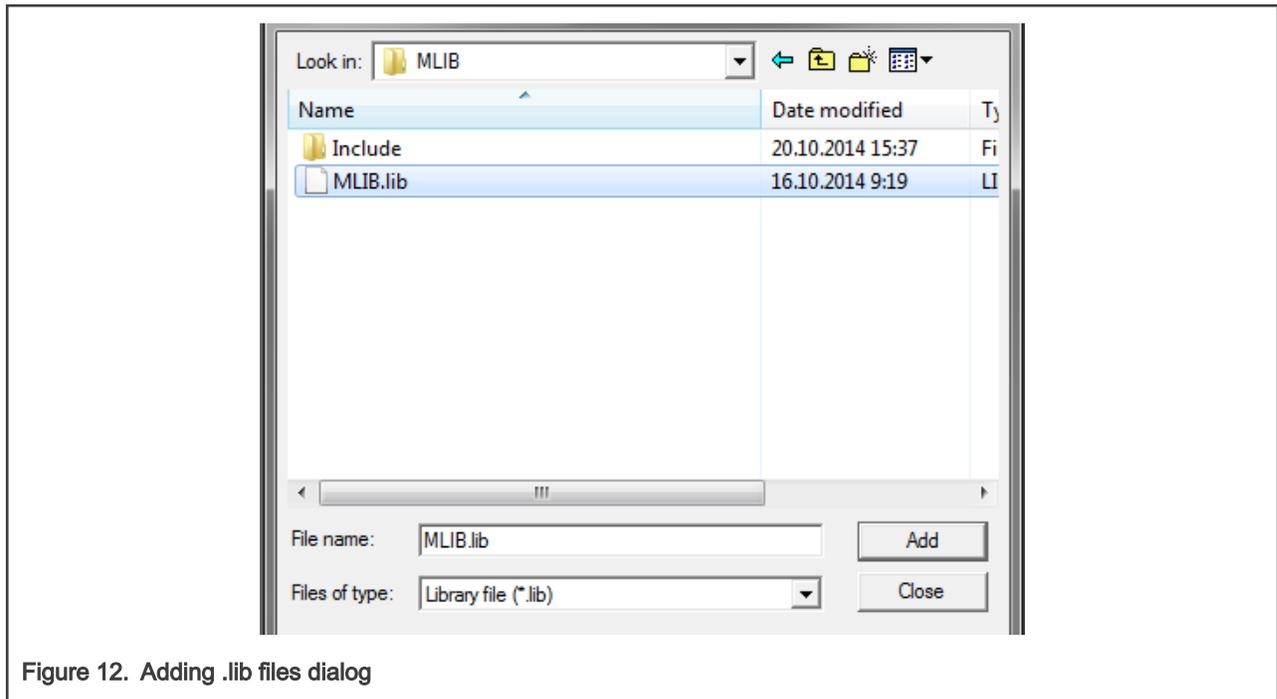


Figure 12. Adding .lib files dialog

- Navigate into the library installation folder C:\NXP\RTCESL\CM0_RTCESEL_4.7_KEIL\GFLIB\Include, and select the *gflib.h* file. If the file does not appear, set the Files of type filter to Text file. Click Add.
- Navigate to the parent folder C:\NXP\RTCESL\CM0_RTCESEL_4.7_KEIL\GFLIB, and select the *gflib.lib* file. If the file does not appear, set the Files of type filter to Library file. Click Add.
- Navigate into the library installation folder C:\NXP\RTCESL\CM0_RTCESEL_4.7_KEIL\GMCLIB\Include, and select the *gmclib.h* file. If the file does not appear, set the Files of type filter to Text file. Click Add.

9. Navigate to the parent folder `C:\NXP\RTCESL\CM0_RTCESL_4.7_KEIL\GMCLIB`, and select the `gmclib.lib` file. If the file does not appear, set the Files of type filter to Library file. Click Add.
10. Now, all necessary files are in the project tree; see [Figure 13](#). Click Close.

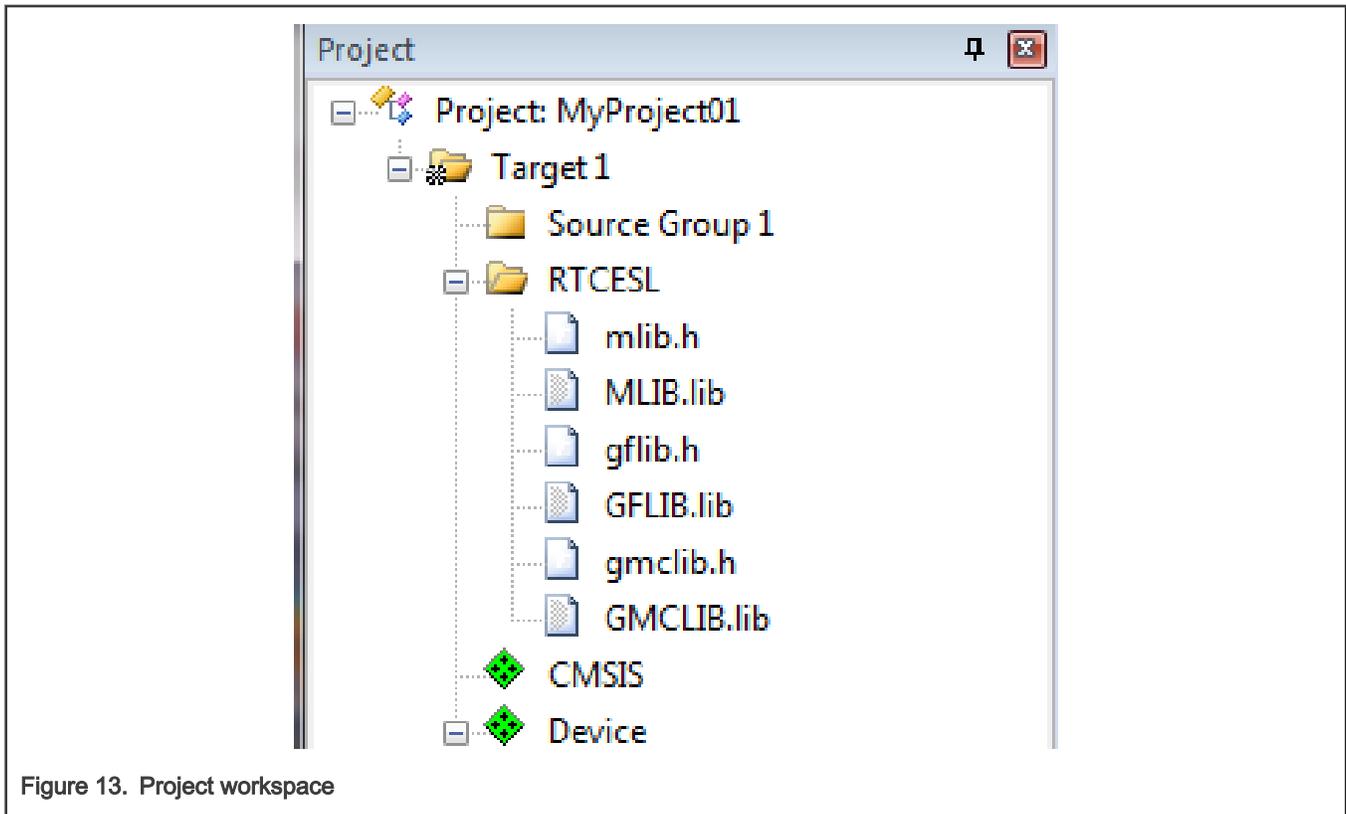


Figure 13. Project workspace

Library path setup

The following steps show the inclusion of all dependent modules.

1. In the main menu, go to Project > Options for Target 'Target1'..., and a dialog appears.
2. Select the C/C++ tab. See [Figure 14](#).
3. In the Include Paths text box, type the following paths (if there are more paths, they must be separated by ';') or add them by clicking the ... button next to the text box:
 - "C:\NXP\RTCESL\CM0_RTCESL_4.7_KEIL\MLIB\Include"
 - "C:\NXP\RTCESL\CM0_RTCESL_4.7_KEIL\GFLIB\Include"
 - "C:\NXP\RTCESL\CM0_RTCESL_4.7_KEIL\GMCLIB\Include"
4. Click OK.
5. Click OK in the main dialog.

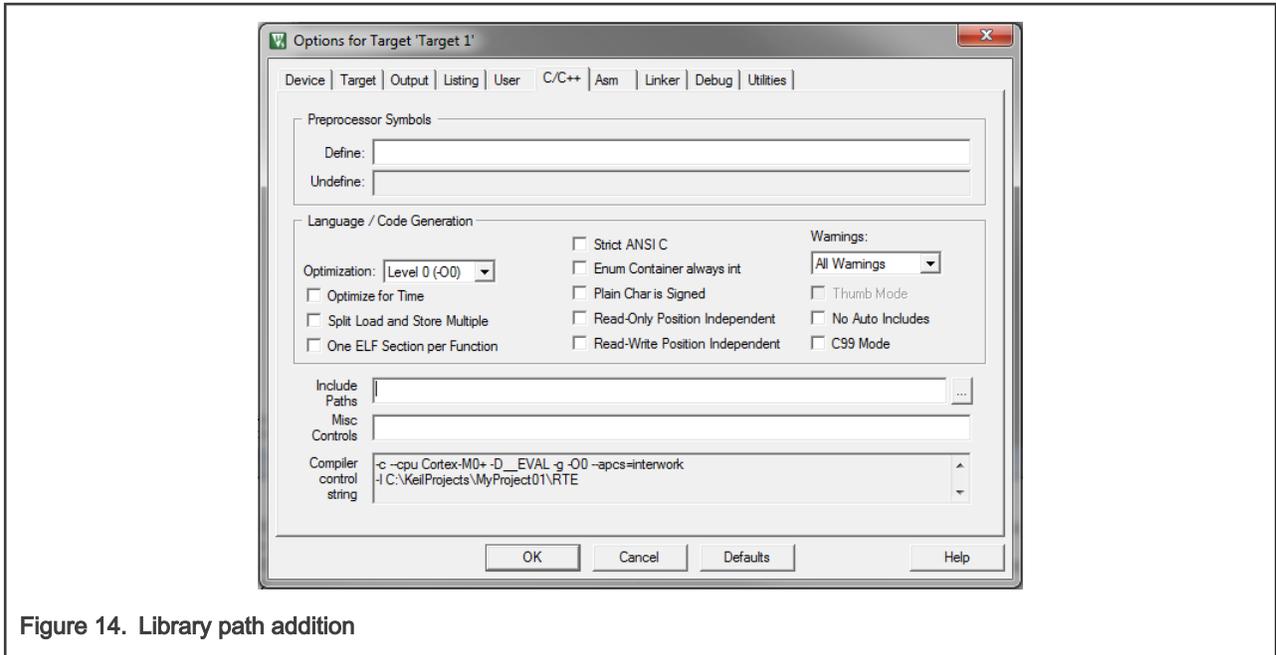


Figure 14. Library path addition

Type the #include syntax into the code. Include the library into a source file. In the new project, it is necessary to create a source file:

1. Right-click the Source Group 1 node, and Add New Item to Group 'Source Group 1'... from the menu.
2. Select the C File (.c) option, and type a name of the file into the Name box, for example 'main.c'. See Figure 15.

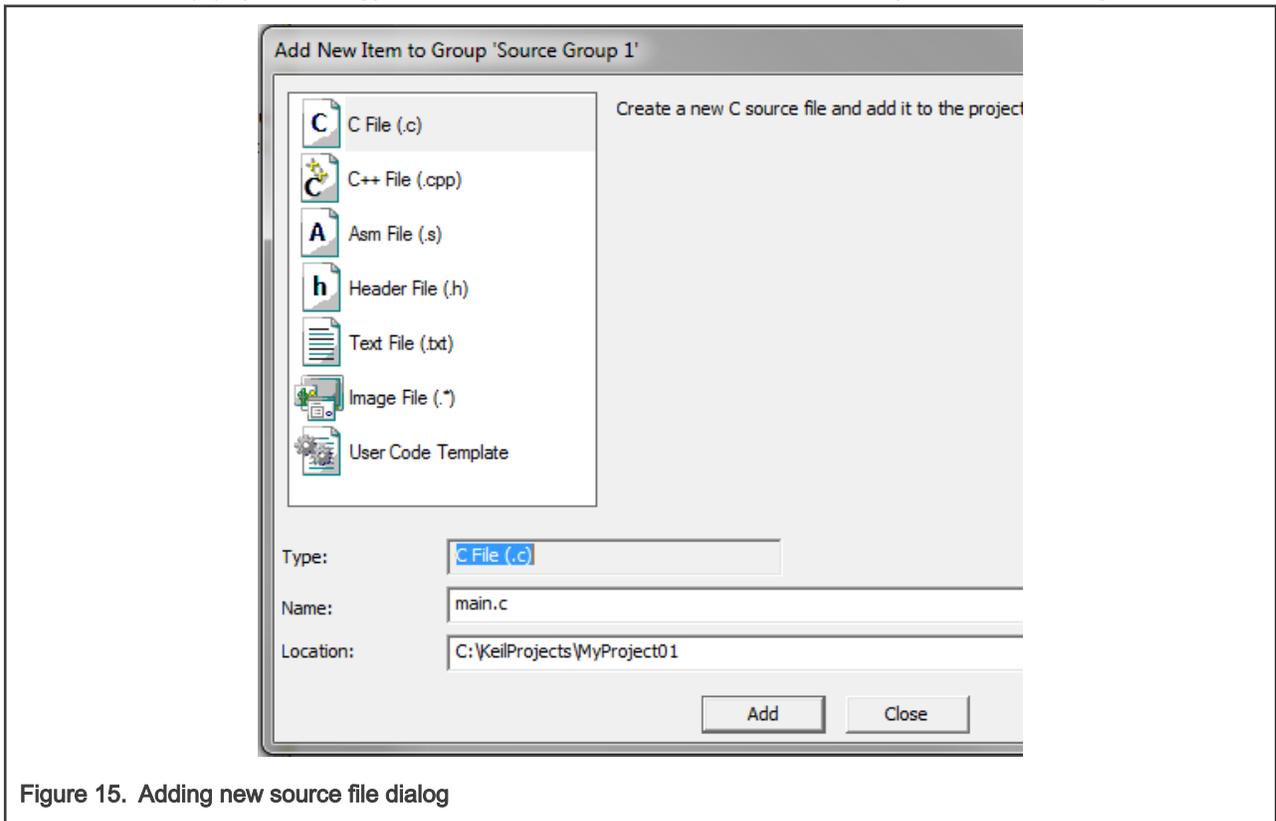


Figure 15. Adding new source file dialog

3. Click Add, and a new source file is created and opened up.

4. In the opened source file, include the following lines into the #include section, and create a main function:

```
#include "mlib.h"
#include "gflib.h"
#include "gmclib.h"

int main(void)
{
    while(1);
}
```

When you click the Build (F7) icon, the project will be compiled without errors.

1.4 Library integration into project (IAR Embedded Workbench)

This section provides a step-by-step guide on how to quickly and easily include the GMCLIB into an empty project or any MCUXpresso SDK example or demo application projects using IAR Embedded Workbench. This example uses the default installation path (C:\NXP\RTCESL\CM0_RTCESEL_4.7_IAR). If you have a different installation path, use that path instead. If any MCUXpresso SDK project is intended to use (for example hello_world project) go to [Memory-mapped divide and square root support](#) chapter otherwise read next chapter.

New project (without MCUXpresso SDK)

This example uses the NXP MKV10Z32xxx7 part, and the default installation path (C:\NXP\RTCESL\CM0_RTCESEL_4.7_IAR) is supposed. To start working on an application, create a new project. If the project already exists and is opened, skip to the next section. Perform these steps to create a new project:

1. Launch IAR Embedded Workbench.
2. In the main menu, select Project > Create New Project... so that the "Create New Project" dialog appears. See [Figure 16](#).

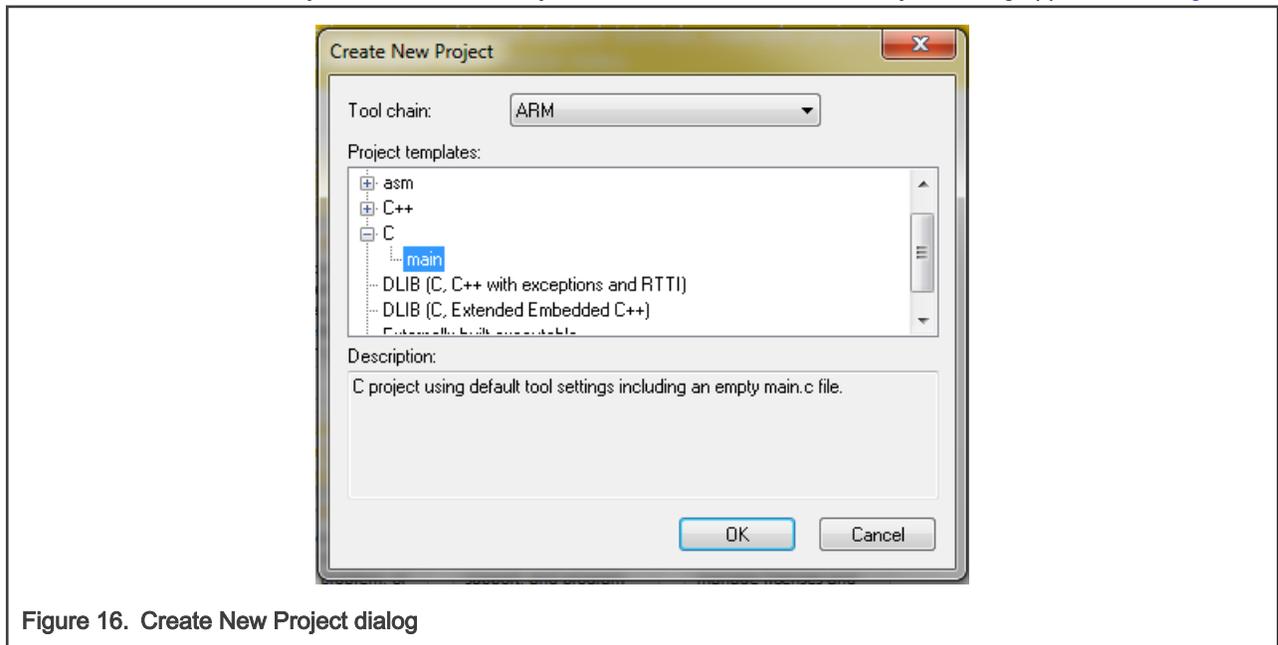


Figure 16. Create New Project dialog

3. Expand the C node in the tree, and select the "main" node. Click OK.
4. Navigate to the folder where you want to create the project, for example, C:\IARProjects\MyProject01. Type the name of the project, for example, MyProject01. Click Save, and a new project is created. The new project is now visible in the left-hand part of IAR Embedded Workbench. See [Figure 17](#).

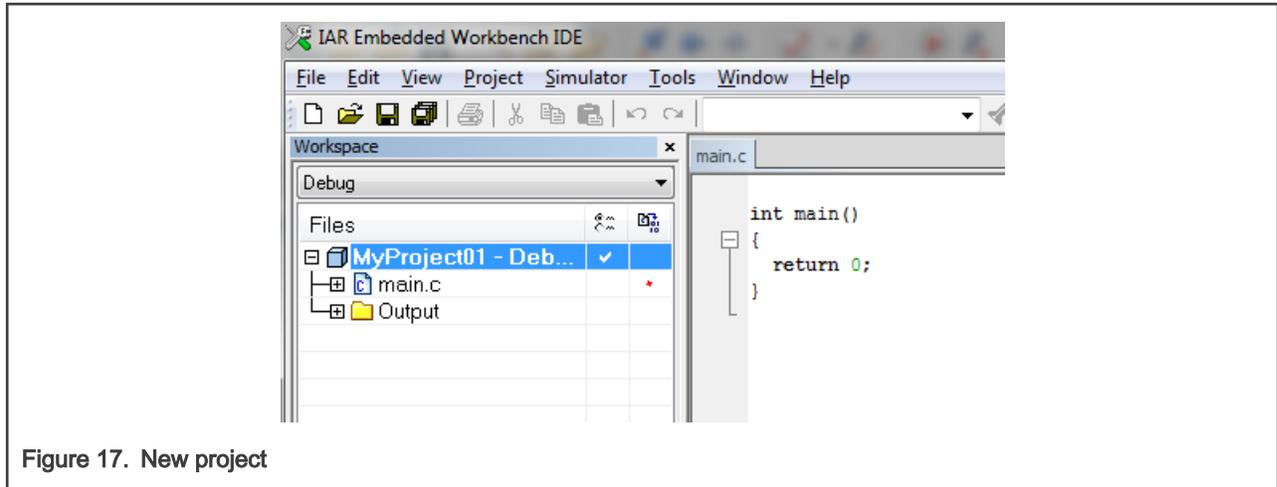


Figure 17. New project

5. In the main menu, go to Project > Options..., and a dialog appears.
6. In the Target tab, select the Device option, and click the button next to the dialog to select the MCU. In this example, select NXP > KV1x > NXP MKV10Z32xxx7. Click OK. See Figure 18.

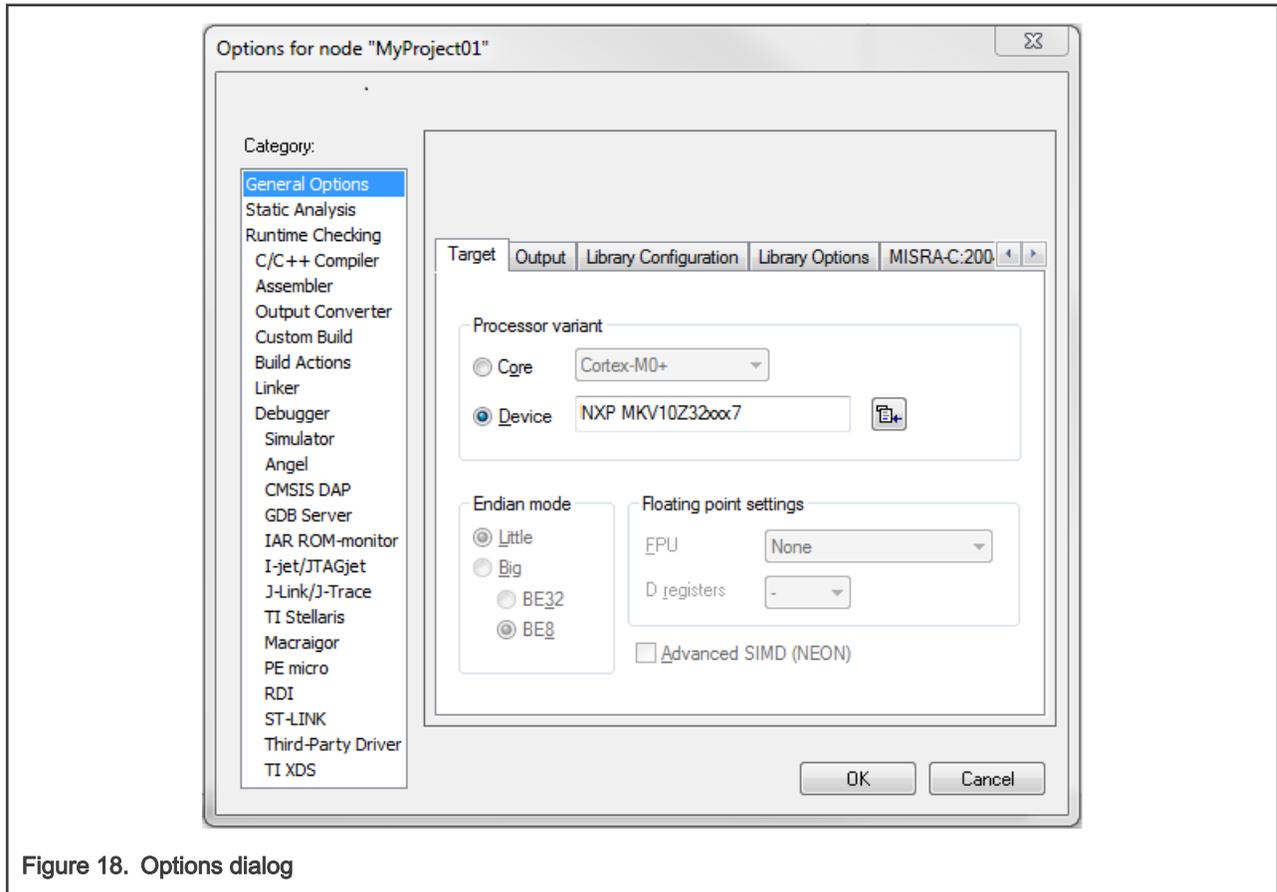


Figure 18. Options dialog

Memory-mapped divide and square root support

Some Kinetis platforms contain a peripheral module dedicated to division and square root. This section shows how to turn the memory-mapped divide and square root (MMDV SQ) support on and off.

1. In the main menu, go to Project > Options..., and a dialog appears.
2. In the left-hand column, select C/C++ Compiler.

3. In the right-hand part of the dialog, click the Preprocessor tab (it can be hidden in the right; use the arrow icons for navigation).
4. In the text box (at the Defined symbols: (one per line)), type the following (See [Figure 19](#)):
 - RTCESL_MMDVSQ_ON—to turn the hardware division and square root support on
 - RTCESL_MMDVSQ_OFF—to turn the hardware division and square root support off

If neither of these two defines is defined, the hardware division and square root support is turned off by default.

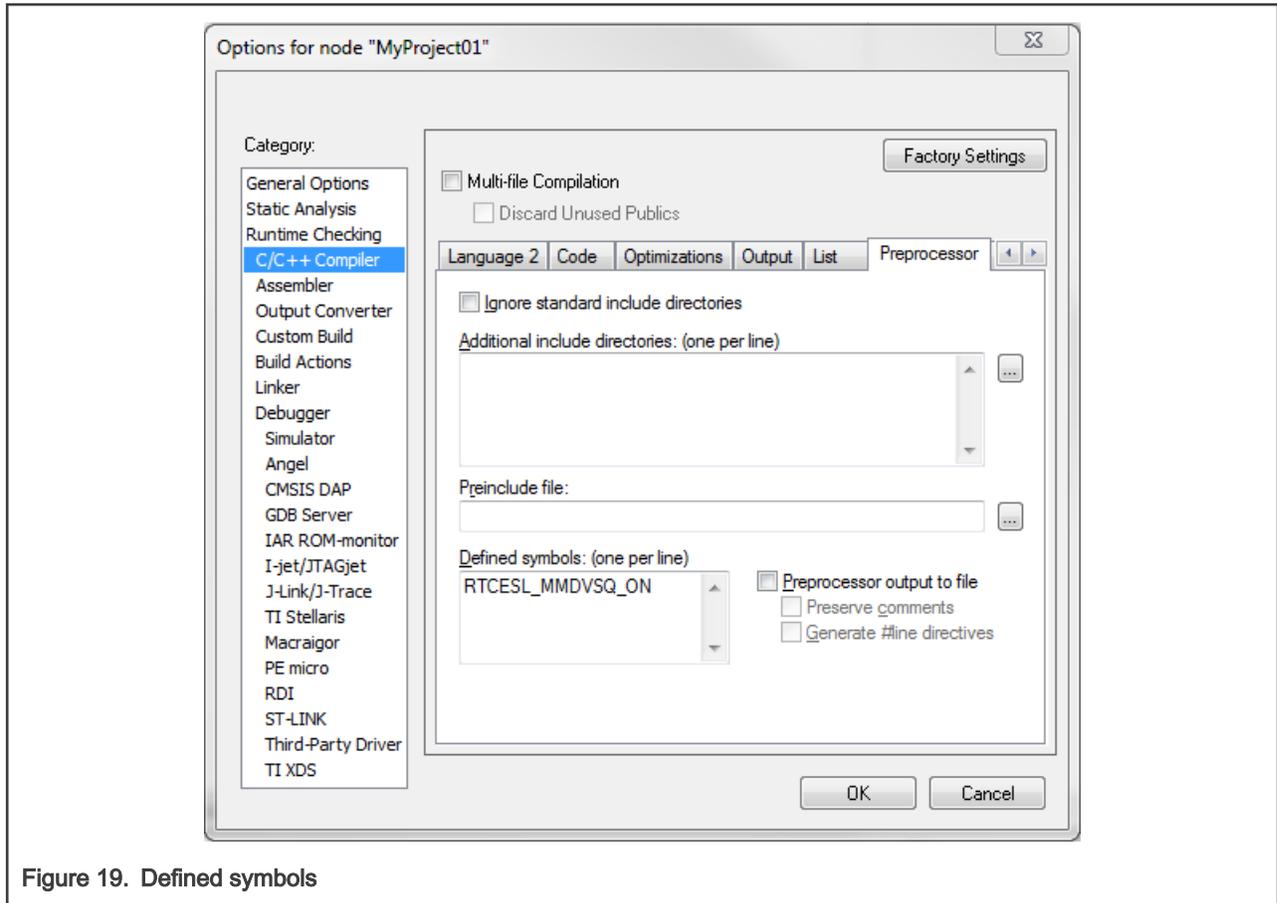


Figure 19. Defined symbols

5. Click OK in the main dialog.

See the device reference manual to verify whether the device contains the MMDVSQ module.

Library path variable

To make the library integration easier, create a variable that will hold the information about the library path.

1. In the main menu, go to Tools > Configure Custom Argument Variables..., and a dialog appears.
2. Click the New Group button, and another dialog appears. In this dialog, type the name of the group PATH, and click OK. See [Figure 20](#).

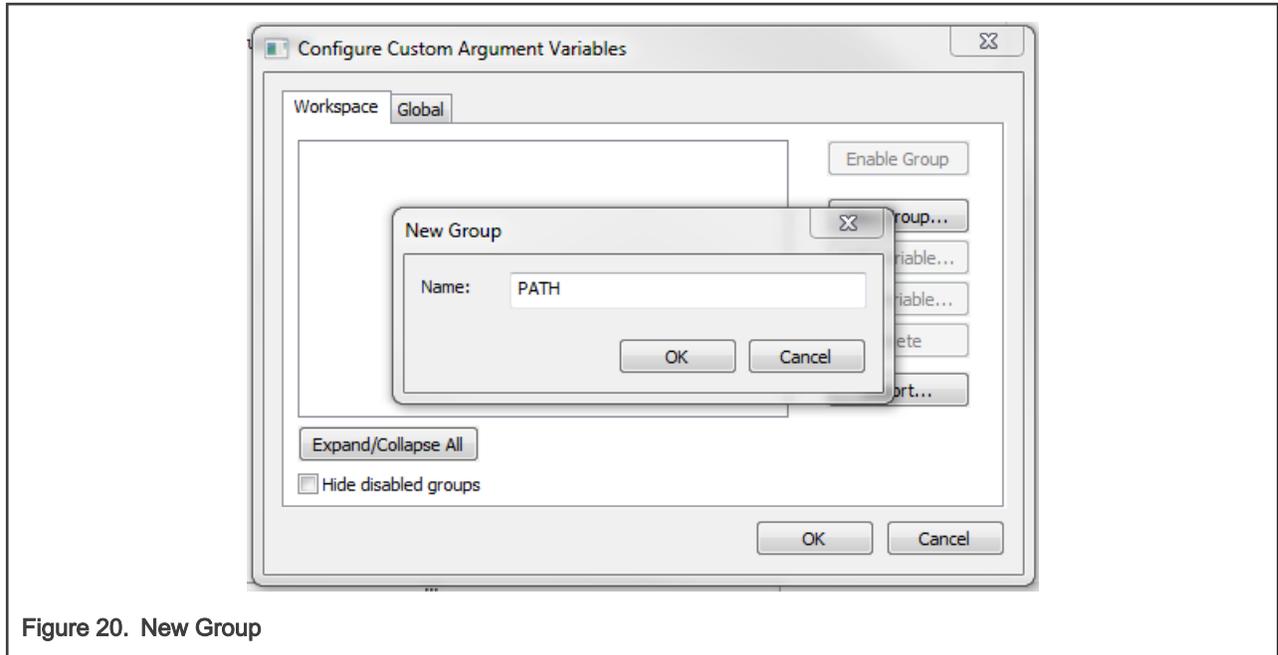


Figure 20. New Group

3. Click on the newly created group, and click the Add Variable button. A dialog appears.
4. Type this name: RTCESL_LOC
5. To set up the value, look for the library by clicking the '...' button, or just type the installation path into the box: C:\NXP\RTCESL\CM0_RTCESL_4.7_IAR. Click OK.
6. In the main dialog, click OK. See [Figure 21](#).

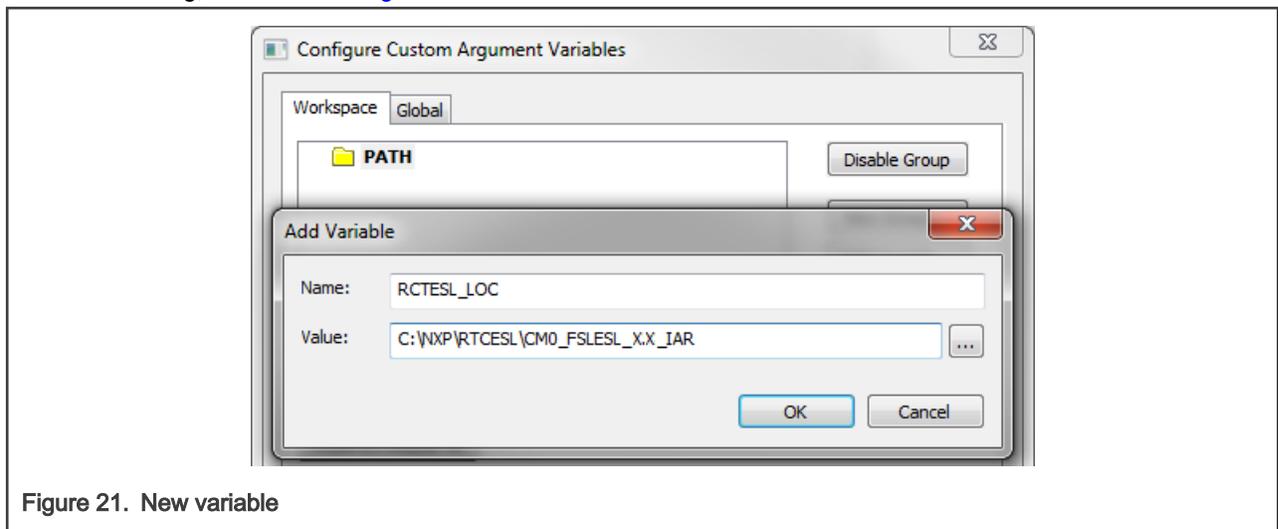


Figure 21. New variable

Linking the files into the project

GMCLIB requires MLIB and GFLIB to be included too. The following steps show the inclusion of all dependent modules.

To include the library files into the project, create groups and add them.

1. Go to the main menu Project > Add Group...
2. Type RTCESL, and click OK.
3. Click on the newly created node RTCESL, go to Project > Add Group..., and create a MLIB subgroup.
4. Click on the newly created node MLIB, and go to the main menu Project > Add Files... See [Figure 23](#).

- Navigate into the library installation folder C:\NXP\RTCESL\CM0_RTCESEL_4.7_IAR\MLIB\Include, and select the *mlib.h* file. (If the file does not appear, set the file-type filter to Source Files.) Click Open. See [Figure 22](#).
- Navigate into the library installation folder C:\NXP\RTCESL\CM0_RTCESEL_4.7_IAR\MLIB, and select the *mlib.a* file. If the file does not appear, set the file-type filter to Library / Object files. Click Open.

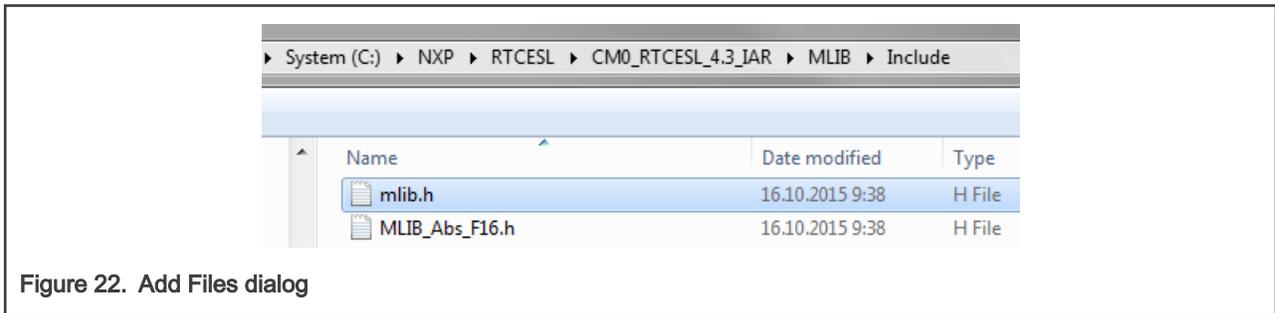


Figure 22. Add Files dialog

- Click on the RTCESL node, go to Project > Add Group..., and create a GFLIB subgroup.
- Click on the newly created node GFLIB, and go to the main menu Project > Add Files....
- Navigate into the library installation folder C:\NXP\RTCESL\CM0_RTCESEL_4.7_IAR\GFLIB\Include, and select the *gflib.h* file. (If the file does not appear, set the file-type filter to Source Files.) Click Open.
- Navigate into the library installation folder C:\NXP\RTCESL\CM0_RTCESEL_4.7_IAR\GFLIB, and select the *gflib.a* file. If the file does not appear, set the file-type filter to Library / Object files. Click Open.
- Click on the RTCESL node, go to Project > Add Group..., and create a GMCLIB subgroup.
- Click on the newly created node GMCLIB, and go to the main menu Project > Add Files....
- Navigate into the library installation folder C:\NXP\RTCESL\CM0_RTCESEL_4.7_IAR\GMCLIB\Include, and select the *gmclib.h* file. If the file does not appear, set the file-type filter to Source Files. Click Open.
- Navigate into the library installation folder C:\NXP\RTCESL\CM0_RTCESEL_4.7_IAR\GMCLIB, and select the *gmclib.a* file. If the file does not appear, set the file-type filter to Library / Object files. Click Open.
- Now you will see the files added in the workspace. See [Figure 23](#).

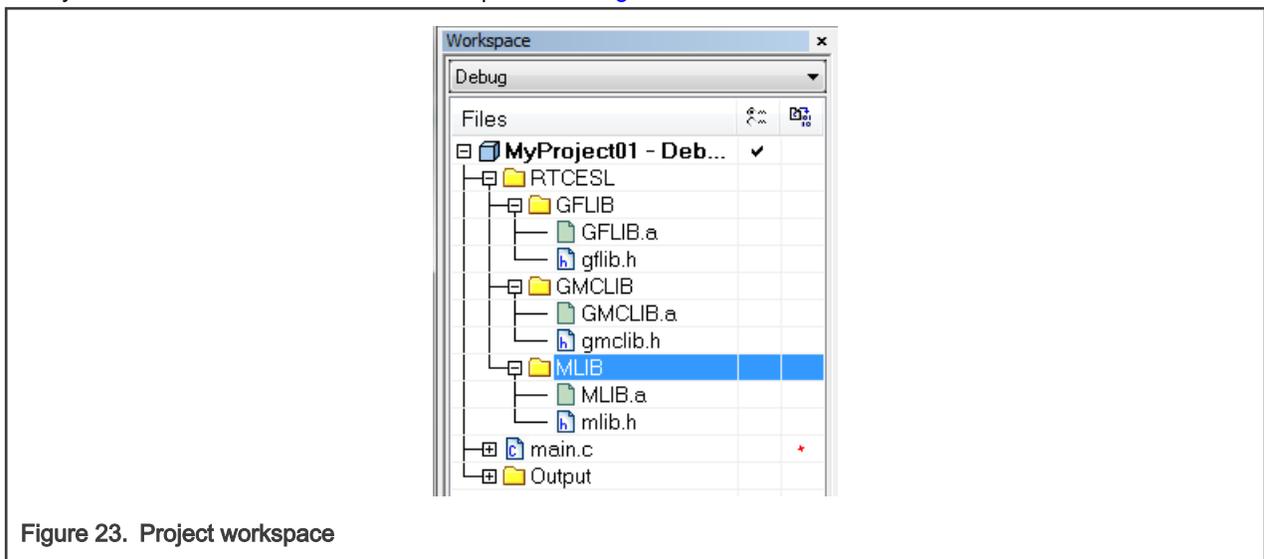


Figure 23. Project workspace

Library path setup

The following steps show the inclusion of all dependent modules:

- In the main menu, go to Project > Options..., and a dialog appears.

2. In the left-hand column, select C/C++ Compiler.
3. In the right-hand part of the dialog, click on the Preprocessor tab (it can be hidden in the right; use the arrow icons for navigation).
4. In the text box (at the Additional include directories title), type the following folder (using the created variable):
 - \$RTCESL_LOC\$\MLIB\Include
 - \$RTCESL_LOC\$\GFLIB\Include
 - \$RTCESL_LOC\$\GMCLIB\Include
5. Click OK in the main dialog. See [Figure 24](#).

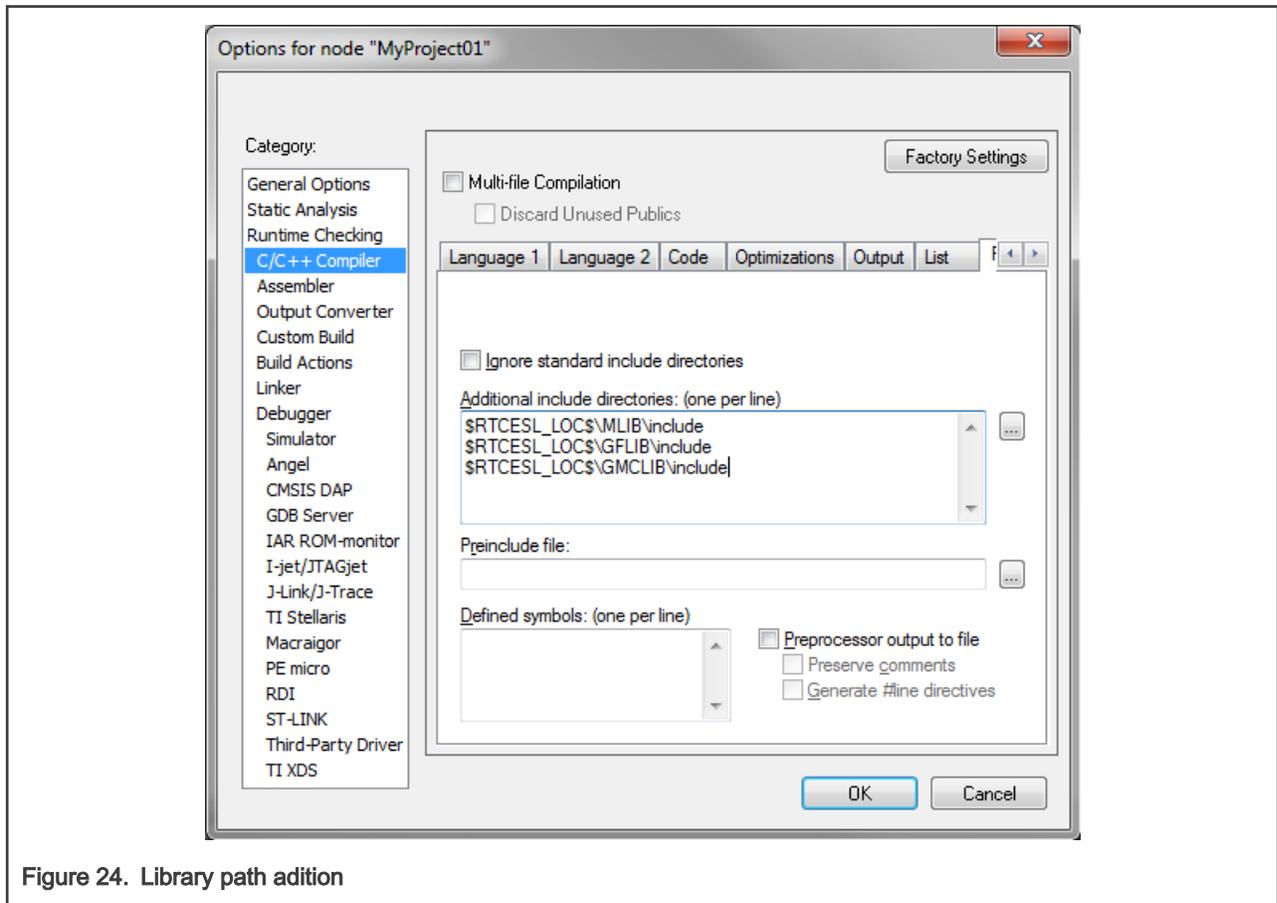


Figure 24. Library path addition

Type the `#include` syntax into the code. Include the library included into the `main.c` file. In the workspace tree, double-click the `main.c` file. After the `main.c` file opens up, include the following lines into the `#include` section:

```
#include "mlib.h"
#include "gflib.h"
#include "gmclib.h"
```

When you click the Make icon, the project will be compiled without errors.

Chapter 2

Algorithms in detail

2.1 GMCLIB_Clark

The [GMCLIB_Clark](#) function calculates the Clarke transformation, which is used to transform values (flux, voltage, current) from the three-phase coordinate system to the two-phase (α - β) orthogonal coordinate system, according to the following equations:

$\alpha = a$
$\beta = \frac{1}{\sqrt{3}}b - \frac{1}{\sqrt{3}}c$

2.1.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range $<-1 ; 1$). The result may saturate.

The available versions of the [GMCLIB_Clark](#) function are shown in the following table:

Table 2. Function versions

Function name	Input type	Output type	Result type
GMCLIB_Clark_F16	GMCLIB_3COOR_T_F16 *	GMCLIB_2COOR_ALBE_T_F16 *	void
	Clarke transformation of a 16-bit fractional three-phase system input to a 16-bit fractional two-phase system. The input and output are within the fractional range $<-1 ; 1$).		

2.1.2 Declaration

The available [GMCLIB_Clark](#) functions have the following declarations:

```
void GMCLIB_Clark_F16(const GMCLIB\_3COOR\_T\_F16 *psIn, GMCLIB\_2COOR\_ALBE\_T\_F16 *psOut)
```

2.1.3 Function use

The use of the [GMCLIB_Clark](#) function is shown in the following examples:

```
Fixed-point version:

#include "gmclib.h"

static GMCLIB\_2COOR\_ALBE\_T\_F16 sAlphaBeta;
static GMCLIB\_3COOR\_T\_F16 sAbc;

void Isr(void);

void main(void)
{
    /* ABC structure initialization */
    sAbc.f16A = FRAC16(0.0);
    sAbc.f16B = FRAC16(0.0);
    sAbc.f16C = FRAC16(0.0);
}
```

```

}

/* Periodical function or interrupt */
void Isr(void)
{
    /* Clarke Transformation calculation */
    GMCLIB_Clark_F16(&sAbc, &sAlphaBeta);
}
    
```

2.2 GMCLIB_ClarkInv

The [GMCLIB_ClarkInv](#) function calculates the Clarke transformation, which is used to transform values (flux, voltage, current) from the two-phase (α - β) orthogonal coordinate system to the three-phase coordinate system, according to the following equations:

$a = \alpha$
$b = -\frac{1}{2}\alpha + \frac{\sqrt{3}}{2}\beta$
$c = -(a + b)$

2.2.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range $<-1 ; 1$). The result may saturate.

The available versions of the [GMCLIB_ClarkInv](#) function are shown in the following table:

Table 3. Function versions

Function name	Input type	Output type	Result type
GMCLIB_ClarkInv_F16	GMCLIB_2COOR_ALBE_T_F16 *	GMCLIB_3COOR_T_F16 *	void
	Inverse Clarke transformation with a 16-bit fractional two-phase system input and a 16-bit fractional three-phase output. The input and output are within the fractional range $<-1 ; 1$).		

2.2.2 Declaration

The available [GMCLIB_ClarkInv](#) functions have the following declarations:

```

void GMCLIB_ClarkInv_F16(const GMCLIB\_2COOR\_ALBE\_T\_F16 *psIn, GMCLIB\_3COOR\_T\_F16 *psOut)
    
```

2.2.3 Function use

The use of the [GMCLIB_ClarkInv](#) function is shown in the following examples:

Fixed-point version:

```

#include "gmclib.h"

static GMCLIB\_2COOR\_ALBE\_T\_F16 sAlphaBeta;
static GMCLIB\_3COOR\_T\_F16 sAbc;
    
```

```

void Isr(void);

void main(void)
{
    /* Alpha, Beta structure initialization */
    sAlphaBeta.f16Alpha = FRAC16(0.0);
    sAlphaBeta.f16Beta = FRAC16(0.0);
}

/* Periodical function or interrupt */
void Isr(void)
{
    /* Inverse Clarke Transformation calculation */
    GMCLIB_ClarkInv_F16(&sAlphaBeta, &sAbc);
}

```

2.3 GMCLIB_Park

The [GMCLIB_Park](#) function calculates the Park transformation, which transforms values (flux, voltage, current) from the stationary two-phase (α - β) orthogonal coordinate system to the rotating two-phase (d-q) orthogonal coordinate system, according to the following equations:

$$d = \alpha \cdot \cos(\theta) + \beta \cdot \sin(\theta)$$

$$q = \beta \cdot \cos(\theta) - \alpha \cdot \sin(\theta)$$

where:

- θ is the position (angle)

2.3.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range $<-1 ; 1$). The result may saturate.

The available versions of the [GMCLIB_Park](#) function are shown in the following table:

Table 4. Function versions

Function name	Input type	Output type	Result type
GMCLIB_Park_F16	GMCLIB_2COOR_ALBE_T_F16 *	GMCLIB_2COOR_DQ_T_F16 *	void
	GMCLIB_2COOR_SINCOS_T_F16 *		
The Park transformation of a 16-bit fractional two-phase stationary system input to a 16-bit fractional two-phase rotating system, using a 16-bit fractional angle two-component (sin / cos) position information. The inputs and the output are within the fractional range $<-1 ; 1$).			

2.3.2 Declaration

The available [GMCLIB_Park](#) functions have the following declarations:

```

void GMCLIB_Park_F16(const GMCLIB\_2COOR\_ALBE\_T\_F16 *psIn, const GMCLIB\_2COOR\_SINCOS\_T\_F16
*psAnglePos, GMCLIB\_2COOR\_DQ\_T\_F16 *psOut)

```

2.3.3 Function use

The use of the [GMCLIB_Park](#) function is shown in the following examples:

Fixed-point version:

```
#include "gmclib.h"

static GMCLIB_2COOR_ALBE_T_F16 sAlphaBeta;
static GMCLIB_2COOR_DQ_T_F16 sDQ;
static GMCLIB_2COOR_SINCOS_T_F16 sAngle;

void Isr(void);

void main(void)
{
    /* Alpha, Beta structure initialization */
    sAlphaBeta.f16Alpha = FRAC16(0.0);
    sAlphaBeta.f16Beta = FRAC16(0.0);

    /* Angle structure initialization */
    sAngle.f16Sin = FRAC16(0.0);
    sAngle.f16Cos = FRAC16(1.0);
}

/* Periodical function or interrupt */
void Isr(void)
{
    /* Park Transformation calculation */
    GMCLIB_Park_F16(&sAlphaBeta, &sAngle, &sDQ);
}
```

2.4 GMCLIB_ParkInv

The [GMCLIB_ParkInv](#) function calculates the Park transformation, which transforms values (flux, voltage, current) from the rotating two-phase (d-q) orthogonal coordinate system to the stationary two-phase (α - β) coordinate system, according to the following equations:

$$\alpha = d \cdot \cos(\theta) - q \cdot \sin(\theta)$$

$$\beta = d \cdot \sin(\theta) + q \cdot \cos(\theta)$$

where:

- θ is the position (angle)

2.4.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range $<-1 ; 1$). The result may saturate.

The available versions of the [GMCLIB_ParkInv](#) function are shown in the following table:

Table 5. Function versions

Function name	Input type	Output type	Result type
GMCLIB_ParkInv_F16	GMCLIB_2COOR_DQ_T_F16 *	GMCLIB_2COOR_ALBE_T_F16 *	void
	GMCLIB_2COOR_SINCOS_T_F16 *		
Inverse Park transformation of a 16-bit fractional two-phase rotating system input to a 16-bit fractional two-phase stationary system, using a 16-bit fractional angle two-component (sin / cos) position information. The inputs and the output are within the fractional range <-1 ; 1).			

2.4.2 Declaration

The available [GMCLIB_ParkInv](#) functions have the following declarations:

```
void GMCLIB_ParkInv_F16(const GMCLIB\_2COOR\_DQ\_T\_F16 *psIn, const GMCLIB\_2COOR\_SINCOS\_T\_F16
*psAnglePos, GMCLIB\_2COOR\_ALBE\_T\_F16 *psOut)
```

2.4.3 Function use

The use of the [GMCLIB_ParkInv](#) function is shown in the following examples:

Fixed-point version:

```
#include "gmclib.h"

static GMCLIB\_2COOR\_ALBE\_T\_F16 sAlphaBeta;
static GMCLIB\_2COOR\_DQ\_T\_F16 sDQ;
static GMCLIB\_2COOR\_SINCOS\_T\_F16 sAngle;

void Isr(void);

void main(void)
{
    /* D, Q structure initialization */
    sDQ.f16D = FRAC16(0.0);
    sDQ.f16Q = FRAC16(0.0);

    /* Angle structure initialization */
    sAngle.f16Sin = FRAC16(0.0);
    sAngle.f16Cos = FRAC16(1.0);
}

/* Periodical function or interrupt */
void Isr(void)
{
    /* Inverse Park Transformation calculation */
    GMCLIB_ParkInv_F16(&sDQ, &sAngle, &sAlphaBeta);
}
```

2.5 GMCLIB_DecouplingPMSM

The [GMCLIB_DecouplingPMSM](#) function calculates the cross-coupling voltages to eliminate the d-q axis coupling that causes nonlinearity of the control.

The d-q model of the motor contains cross-coupling voltage that causes nonlinearity of the control. [Figure 1](#) represents the d-q model of the motor that can be described using the following equations, where the underlined portion is the cross-coupling voltage:

$$u_d = R_s \cdot i_d + L_d \frac{d}{dt} i_d + \underline{L_q \cdot \omega_{el} \cdot i_q}$$

$$u_q = R_s \cdot i_q + L_q \frac{d}{dt} i_q - \underline{L_d \cdot \omega_{el} \cdot i_d} + \omega_{el} \cdot \psi_r$$

where:

- u_d, u_q are the d and q voltages
- i_d, i_q are the d and q currents
- R_s is the stator winding resistance
- L_d, L_q are the stator winding d and q inductances
- ω_{el} is the electrical angular speed
- ψ_r is the rotor flux constant

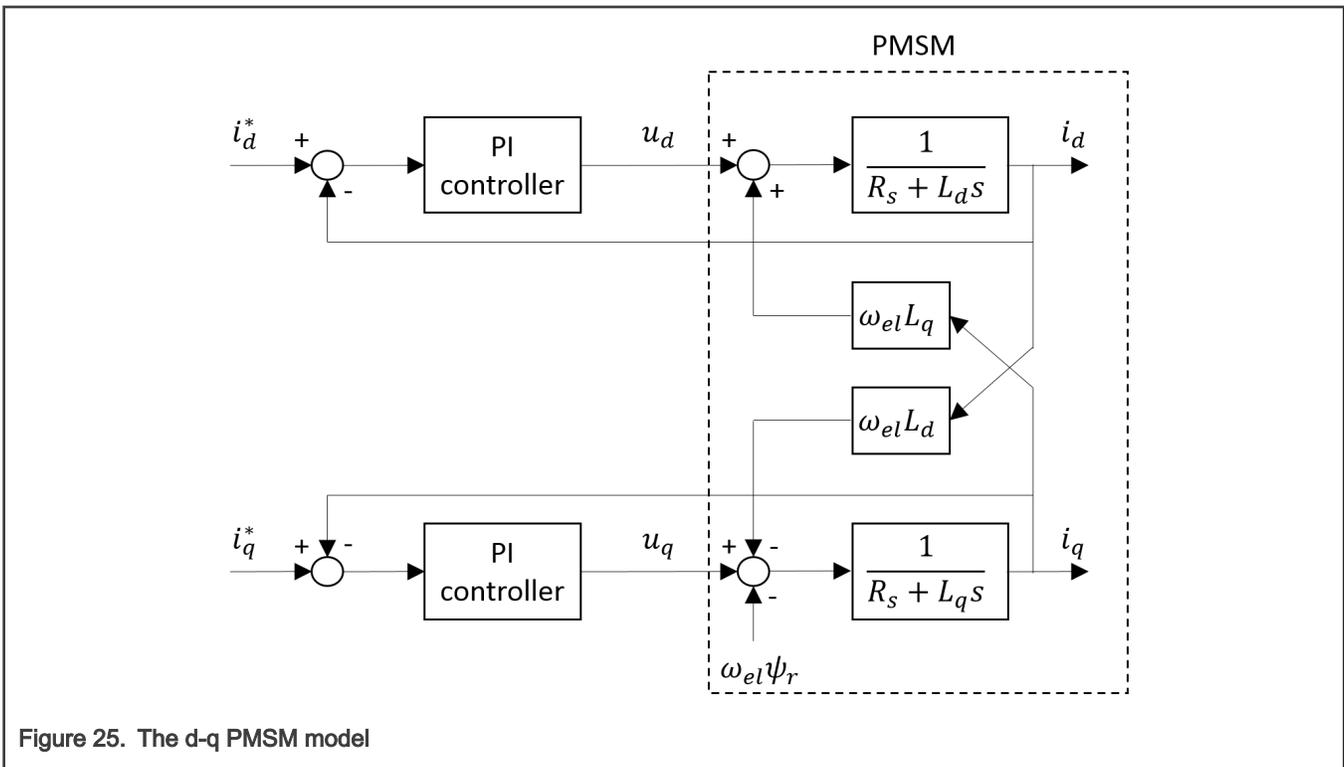


Figure 25. The d-q PMSM model

To eliminate the nonlinearity, the cross-coupling voltage is calculated using the [GMCLIB_DecouplingPMSM](#) algorithm, and feedforwarded to the d and q voltages. The decoupling algorithm is calculated using the following equations:

$$u_{ddec} = u_d - L_q \cdot \omega_{el} \cdot i_q$$

$$u_{qdec} = u_q + L_d \cdot \omega_{el} \cdot i_d$$

where:

- u_d, u_q are the d and q voltages; inputs to the algorithm

- u_{ddec} , u_{qdec} are the d and q decoupled voltages; outputs from the algorithm

The fractional representation of the d-component equation is as follows:

$$u_{ddec} = u_d - \omega_{el} \cdot i_q \left(L_q \cdot \omega_{el_max} \cdot \frac{i_{max}}{u_{max}} \right)$$

$$k_q = L_q \cdot \omega_{el_max} \cdot \frac{i_{max}}{u_{max}}$$

$$u_{ddec} = u_d - \omega_{el} \cdot i_q \cdot k_q$$

The fractional representation of the q-component equation is as follows:

$$u_{qdec} = u_q + \omega_{el} \cdot i_d \left(L_d \cdot \omega_{el_max} \cdot \frac{i_{max}}{u_{max}} \right)$$

$$k_d = L_d \cdot \omega_{el_max} \cdot \frac{i_{max}}{u_{max}}$$

$$u_{qdec} = u_q + \omega_{el} \cdot i_d \cdot k_d$$

where:

- k_d , k_q are the scaling coefficients
- i_{max} is the maximum current
- u_{max} is the maximum voltage
- ω_{el_max} is the maximum electrical speed

The k_d and k_q parameters must be set up properly.

The principle of the algorithm is depicted in [Figure 2](#):

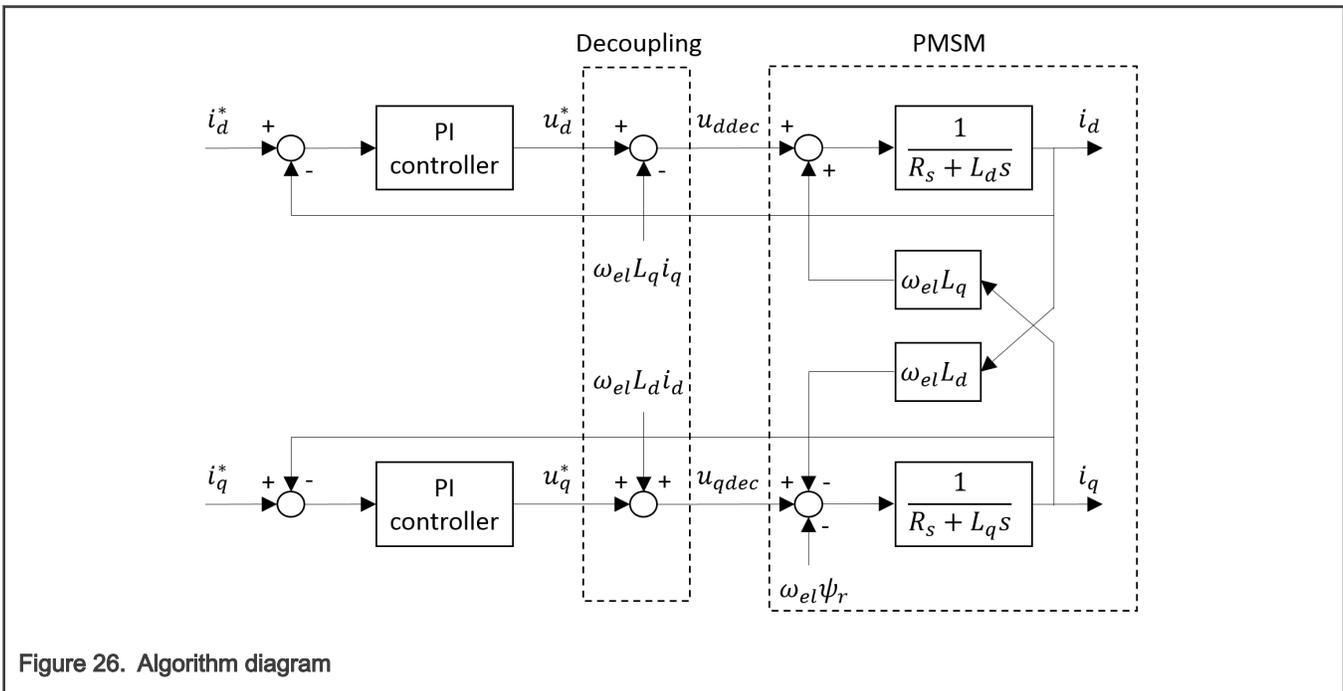


Figure 26. Algorithm diagram

2.5.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range <-1 ; 1). The result may saturate. The parameters use the accumulator types.

The available versions of the [GMCLIB_DecouplingPMSM](#) function are shown in the following table:

Table 6. Function versions

Function name	Input/output type		Result type
GMCLIB_DecouplingPMSM_F16	Input	GMCLIB_2COOR_DQ_T_F16 *	void
		GMCLIB_2COOR_DQ_T_F16 *	
		frac16_t	
	Parameters	GMCLIB_DECOUPLINGPMSM_T_A32 *	
	Output	GMCLIB_2COOR_DQ_T_F16 *	
The PMSM decoupling with a 16-bit fractional d-q voltage, current inputs, and a 16-bit fractional electrical speed input. The parameters are 32-bit accumulator types. The output is a 16-bit fractional decoupled d-q voltage. The inputs and the output are within the range <-1 ; 1).			

2.5.2 GMCLIB_DECOUPLINGPMSM_T_A32 type description

Variable name	Input type	Description
a32KdGain	acc32_t	Direct axis decoupling parameter. The parameter is within the range <0 ; 65536.0)
a32KqGain	acc32_t	Quadrature axis decoupling parameter. The parameter is within the range <0 ; 65536.0)

2.5.3 Declaration

The available [GMCLIB_DecouplingPMSM](#) functions have the following declarations:

```
void GMCLIB_DecouplingPMSM_F16(const GMCLIB_2COOR_DQ_T_F16 *psUDQ, const GMCLIB_2COOR_DQ_T_F16 *psIDQ, frac16_t f16SpeedEl, const GMCLIB_DECOUPLINGPMSM_T_A32 *psParam, GMCLIB_2COOR_DQ_T_F16 *psUDQDec)
```

2.5.4 Function use

The use of the [GMCLIB_DecouplingPMSM](#) function is shown in the following examples:

```
Fixed-point version:

#include "gmclib.h"

static GMCLIB_2COOR_DQ_T_F16 sVoltageDQ;
static GMCLIB_2COOR_DQ_T_F16 sCurrentDQ;
static frac16_t f16AngularSpeed;
static GMCLIB_DECOUPLINGPMSM_T_A32 sDecouplingParam;
static GMCLIB_2COOR_DQ_T_F16 sVoltageDQDecoupled;

void Isr(void);

void main(void)
{
```

```

/* Voltage D, Q structure initialization */
sVoltageDQ.f16D = FRAC16(0.0);
sVoltageDQ.f16Q = FRAC16(0.0);

/* Current D, Q structure initialization */
sCurrentDQ.f16D = FRAC16(0.0);
sCurrentDQ.f16Q = FRAC16(0.0);

/* Speed initialization */
f16AngularSpeed = FRAC16(0.0);

/* Motor parameters for decoupling Kd = 40, Kq = 20 */
sDecouplingParam.a32KdGain = ACC32(40.0);
sDecouplingParam.a32KqGain = ACC32(20.0);
}

/* Periodical function or interrupt */
void Isr(void)
{
    /* Decoupling calculation */
    GMCLIB_DcouplingPMSM_F16(&sVoltageDQ, &sCurrentDQ, f16AngularSpeed,
    &sDecouplingParam, &sVoltageDQDecoupled);
}

```

2.6 GMCLIB_DTCompLut1D

The [GMCLIB_DTCompLut1D](#) function implements dead-time-compensation algorithms that return error voltages from measured currents, knowing the inverter nonlinearity in the Look-Up Table (LUT). The aim of the [GMCLIB_DTCompLut1D](#) function is to make the inverter and the whole control loop more linear, especially around low-duty cycles, where the dead-time effect is dominant. The error voltage obtained from [GMCLIB_DTCompLut1D](#) has the most important impact in the low-motor-speed region, where the motor-supply voltage is low. The next operation is to transform the error voltages from the three-phase (a, b, c) system of coordinates to the two-phase (α , β) orthogonal system using the Clarke transformation. The multiplication by U_{DCBus} voltages is then processed and the output-compensation voltages are obtained after adding input voltages. The principle of the [GMCLIB_DTCompLut1D](#) function is shown in [Figure 27](#).

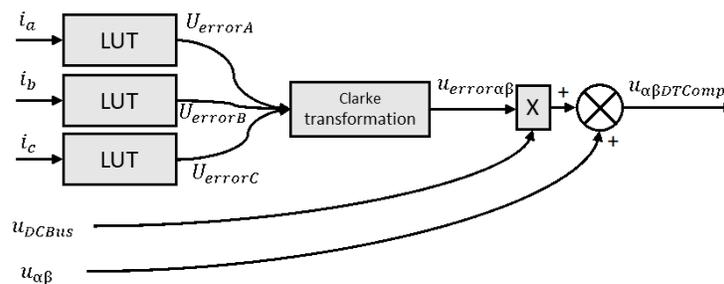


Figure 27. GMCLIB_DTCompLut1D function block scheme

Adding the [GMCLIB_DTCompLut1D](#) function into your application has the following essentials. Each inverter introduces the total error voltage, which is caused by the dead-time and current-clamping effects and the transistor voltage drop. The actual inverter output voltage is lower than the required voltage. The total error voltage depends on the actual phase current. The example of the inverter error characteristic is shown in [Figure 28](#).

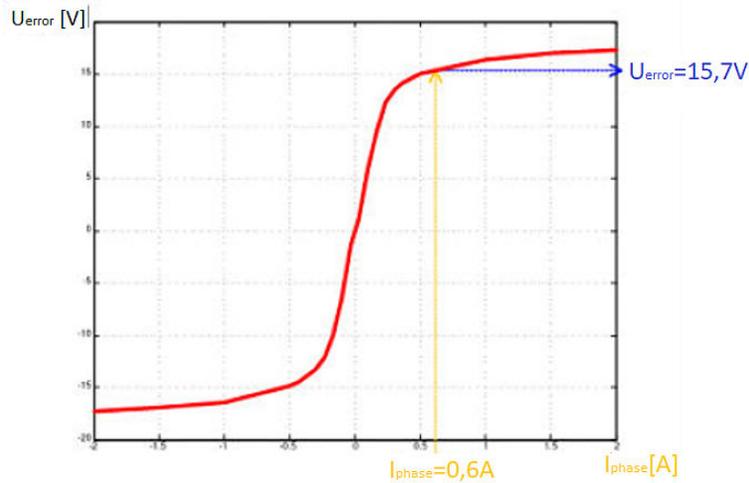


Figure 28. Inverter error characteristic example - voltage error dependency on phase current

The inverter error characteristic is assigned to the [GMCLIB_DTCompLut1D](#) algorithm as the LUT, which simply adds the error-voltage vector to the input-voltage vector. The data for the LUT should be measured from a real inverter for the best compensation result. The target of the measurement is the voltage-error-to-phase-current dependency, as shown in [Figure 29](#).

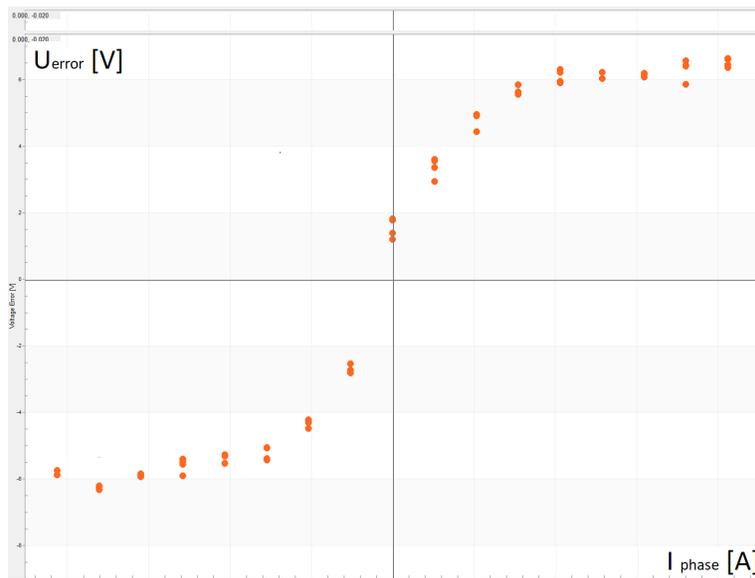


Figure 29. Measured inverter voltage error data example for LUT measured for phase current points

The LUT is defined by the table pointer and tableSize parameters. The table output is the error-voltage vector from the phase-current input vector. The [GMCLIB_DTCompLut1D](#) algorithm processes the compensation voltage according to the following equations:

$$\begin{aligned}
 u_{Aerror} &= GFLIB_Lut1D_F16(i_a, Table, TableSize) \\
 u_{Berror} &= GFLIB_Lut1D_F16(i_b, Table, TableSize) \\
 u_{Cerror} &= GFLIB_Lut1D_F16(i_c, Table, TableSize)
 \end{aligned}$$

Figure 30. Equations to get the error voltages components

where:

- u_{AError} , u_{BError} , and u_{CError} are the error-voltage components of the error-voltage vector.
- i_a , i_b , and i_c are the current components of the measured-current vector.
- The LUT contains the inverter measured characteristic. See [GMCLIB_DTComPLUT1D_T_F16](#) for details.
- The tableSize parameter is the size of the LUT parameter. See [GMCLIB_DTComPLUT1D_T_F16](#) for details.
- The GFLIB_Lut1D_F16 parameter is the LUT function ([GMCLIB_DTCompLut1D](#)).

When the error voltages are calculated, the [GMCLIB_DTCompLut1D](#) algorithm continues using the following equations:

$$u_{\beta DTComp} = u_{\beta} + (2 \times u_{AError} - u_{BError} - u_{CError}) \times \frac{u_{dcbus}}{3}$$

$$u_{\alpha DTComp} = u_{\alpha} + (u_{BError} - u_{CError}) \times \frac{\sqrt{3} \times u_{dcbus}}{3}$$

Figure 31. DTCompLUT1D function equations

where:

- $u_{\alpha DTComp}$ and $u_{\beta DTComp}$ are the compensation voltage components and outputs of the [GMCLIB_DTCompLut1D](#) function.
- u_{α} , and u_{β} are the voltage components of the input-voltage vector.
- u_{AError} , u_{BError} , and u_{CError} are the error-voltage components of the error-voltage vector.
- u_{DCBus} is the DC-Bus voltage.

At the end of the [GMCLIB_DTCompLut1D](#) algorithm, the error-compensation-voltage componenets (α and β) are added to the input voltage components (α and β). The addition with saturation is used to avoid overflow and the results of the [GMCLIB_DTCompLut1D](#) function are the dead-time-compensated voltage components ($U_{\alpha DTComp}$ and $U_{\beta DTComp}$) as inputs for the SVMShifted function.

2.6.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result. The result is in the range of $<-1 ; 1$). The result may saturate. The parameter includes the table and table size used the table types.

Table 7. Function versions

Function name	Input/output type		Result type
GMCLIB_DTCompLut1D_F16	Inputs	GMCLIB_3COOR_T_F16 *, GMCLIB_2COOR_ALBE_T_F16 *, frac16_t	void
	Parameter	GMCLIB_DTComPLUT1D_T_F16 *, *	
	Output	GMCLIB_2COOR_ALBE_T_F16 *	
The first input argument is the structure of current components represented by the 16-bit fractional values. It contains the abscissas for which the 1-D interpolations are performed. The second input argument is the structure of voltage components represented by the two-phase (α , β) orthogonal coordinate system. The last input argument is the measured 16-bit fractional DC-Bus voltage input.			

Table continues on the next page...

Table 7. Function versions

Function name	Input/output type	Result type
	<p>The parameter structure consists of two members of the GMCLIB_DTCOMPLUT1D_T_F16 structure type. The first parameter is the pointer to the LUT and the second parameter is the size of the LUT.</p> <p>The output argument is the structure of compensated voltage components represented by the two-phase (α, β) orthogonal coordinate system, targeted for the SVMShifted function.</p>	

2.6.2 GMCLIB_DTCOMPLUT1D_T_F16 type description

Variable name	Input type	Description
pf16Table	frac16_t *	The pointer to a LUT, which contains the 16-bit fractional values of the LUT.
u16TableSize	uint16_t	The size of the LUT parameter is in the range of <1 ; 15>. It means that the parameter is log2 of the number of points + 1.

2.6.3 Declaration

The available [GMCLIB_DTCompLut1D](#) functions have the following declarations:

```
GMCLIB_DTCompLut1D_F16(const GMCLIB_3COOR_T_F16 *psIABC, const GMCLIB_2COOR_ALBE_T_F16 *psUAlBe,
frac16_t f16UDCbus, const GMCLIB_DTCOMPLUT1D_T_F16 *psParam, GMCLIB_2COOR_ALBE_T_F16 *psUAlBeDTComp)
```

2.6.4 Function use

The use of the [GMCLIB_DTCompLut1D](#) function is shown in the following example:

```
Fixed-point version:

#include "gmclib.h"
static GMCLIB_DTCOMPLUT1D_T_F16 sParam;
static GMCLIB_3COOR_T_F16 sIABC;
static GMCLIB_2COOR_ALBE_T_F16 sUAlBe, sUAlBeComp;
static frac16_t f16UDCbus;
static frac16_t f16Table[9] = {FRAC16(-0.7), FRAC16(-0.65), FRAC16(-0.55),
FRAC16(0.2), FRAC16(0.0),
FRAC16(0.2), FRAC16(-0.8), FRAC16(0.91),
FRAC16(0.99)};
void Isr(void);

void main(void)
{
    /* ABC currents structure initialization */
    sIABC.f16A = FRAC16(0.1);
    sIABC.f16B = FRAC16(0.3);
    sIABC.f16C = FRAC16(-0.2);
    /* Alpha Bete voltages structure initialization */
    sUAlBe.f16Alpha = FRAC16(0.25);
    sUAlBe.f16Beta = FRAC16(0.75);
    /* DC Bus voltage initialization */
```

```

f16UDCbus = FRAC16(0.9);
/* DC Bus voltage initialization */
sParam.pf16Table = f16Table;
sParam.ul6TableSize = 3;
}
/* Periodical function or interrupt */
void Isr(void)
{
/* Dead-Time compensation calculation */
GMCLIB_DTCompLut1D_F16(&sIABC, &sUAlBe, f16UDCbus, &sParam, &sUAlBeComp);
}

```

2.7 GMCLIB_ElimDcBusRipFOC

The [GMCLIB_ElimDcBusRipFOC](#) function is used for the correct PWM duty cycle output calculation, based on the measured DC-bus voltage. The side effect is the elimination of the the DC-bus voltage ripple in the output PWM duty cycle. This function is meant to be used with a space vector modulation, whose modulation index (with respect to the DC-bus voltage) is an inverse square root of 3.

The general equation to calculate the duty cycle for the above-mentioned space vector modulation is as follows:

$$U_{PWM} = \frac{u_{FOC}}{u_{dcbus}} \cdot \sqrt{3}$$

where:

- U_{PWM} is the duty cycle output
- u_{FOC} is the real FOC voltage
- u_{dcbus} is the real measured DC-bus voltage

Using the previous equations, the [GMCLIB_ElimDcBusRipFOC](#) function compensates an amplitude of the direct- α and the quadrature- β component of the stator-reference voltage vector, using the formula shown in the following equations:

$$U_{\alpha}^* = \begin{cases} 0, & U_{\alpha} = 0 \wedge U_{dcbus} = 0 \\ 1, & U_{\alpha} \geq 0 \wedge |U_{\alpha}| \geq \frac{U_{dcbus}}{\sqrt{3}} \\ -1, & U_{\alpha} < 0 \wedge |U_{\alpha}| \geq \frac{U_{dcbus}}{\sqrt{3}} \\ \frac{U_{\alpha}}{U_{dcbus}} \cdot \sqrt{3}, & \text{else} \end{cases}$$

$$U_{\beta}^* = \begin{cases} 0, & U_{\beta} = 0 \wedge U_{dcbus} = 0 \\ 1, & U_{\beta} \geq 0 \wedge |U_{\beta}| \geq \frac{U_{dcbus}}{\sqrt{3}} \\ -1, & U_{\beta} < 0 \wedge |U_{\beta}| \geq \frac{U_{dcbus}}{\sqrt{3}} \\ \frac{U_{\beta}}{U_{dcbus}} \cdot \sqrt{3}, & \text{else} \end{cases}$$

where:

- U_{α}^* is the direct- α duty cycle ratio
- U_{β}^* is the quadrature- β duty cycle ratio
- U_{α} is the direct- α voltage
- U_{β} is the quadrature- β voltage

If the fractional arithmetic is used, the FOC and DC-bus voltages have their scales, which take place in [GMCLIB_ElimDcBusRipFOC_Eq1](#); the equation is as follows:

$$U_{PWM} = \frac{U_{FOC} U_{FOC_max}}{U_{dcbus} U_{dcbus_max}} \cdot \sqrt{3}$$

where:

- U_{FOC} is the scaled FOC voltage
- U_{dcbus} is the scaled measured DC-bus voltage
- U_{FOC_max} is the FOC voltage scale
- U_{dcbus_max} is the DC-bus voltage scale

If this algorithm is used with the space vector modulation with the ratio of square root equal to 3, then the FOC voltage scale is expressed as follows :

$$U_{FOC_max} = \frac{U_{dcbus_max}}{\sqrt{3}}$$

The equation can be simplified as follows:

$$U_{PWM} = \frac{U_{FOC} \frac{U_{dcbus_max}}{\sqrt{3}}}{U_{dcbus} U_{dcbus_max}} \cdot \sqrt{3} = \frac{U_{FOC}}{U_{dcbus}}$$

The [GMCLIB_ElimDcBusRipFOC](#) function compensates an amplitude of the direct- α and the quadrature- β component of the stator-reference voltage vector in the fractional arithmetic, using the formula shown in the following equations:

$$U_{\alpha}^* = \begin{cases} 0, & U_{\alpha} = 0 \wedge U_{dcbus} = 0 \\ 1, & U_{\alpha} > 0 \wedge |U_{\alpha}| \geq U_{dcbus} \\ -1, & U_{\alpha} < 0 \wedge |U_{\alpha}| \geq U_{dcbus} \\ \frac{U_{\alpha}}{U_{dcbus}}, & \text{else} \end{cases}$$

$$U_{\beta}^* = \begin{cases} 0, & U_{\beta} = 0 \wedge U_{dcbus} = 0 \\ 1, & U_{\beta} > 0 \wedge |U_{\beta}| \geq U_{dcbus} \\ -1, & U_{\beta} < 0 \wedge |U_{\beta}| \geq U_{dcbus} \\ \frac{U_{\beta}}{U_{dcbus}}, & \text{else} \end{cases}$$

where:

- U_{α}^* is the direct- α duty cycle ratio
- U_{β}^* is the quadrature- β duty cycle ratio
- U_{α} is the direct- α voltage
- U_{β} is the quadrature- β voltage

The [GMCLIB_ElimDcBusRipFOC](#) function can be used in general motor-control applications, and it provides elimination of the voltage ripple on the DC-bus of the power stage. [Figure 1](#) shows the results of the DC-bus ripple elimination, while compensating the ripples of the rectified voltage using a three-phase uncontrolled rectifier.

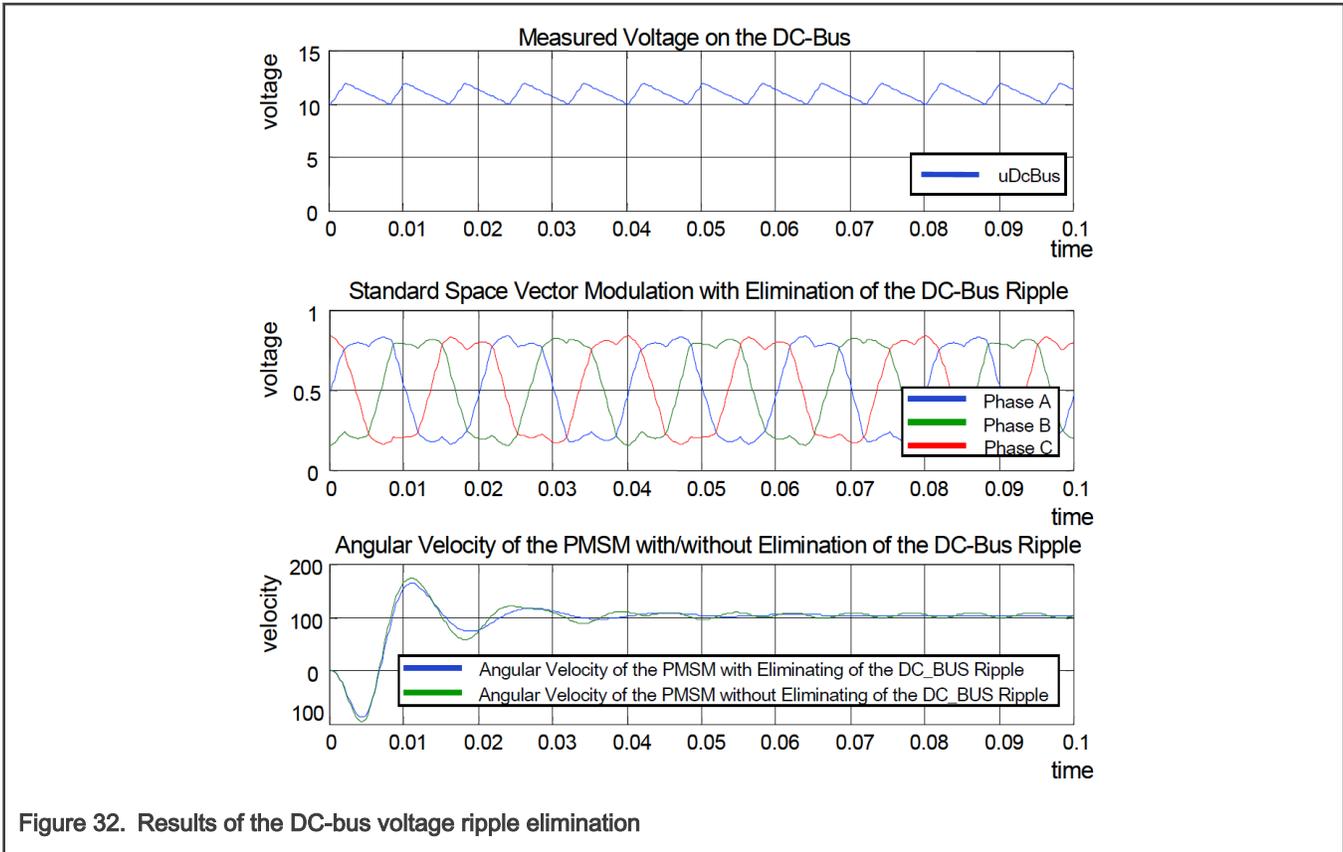


Figure 32. Results of the DC-bus voltage ripple elimination

2.7.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range $<-1 ; 1$). The result may saturate.

The available versions of the [GMCLIB_ElimDcBusRipFOC](#) function are shown in the following table:

Table 8. Function versions

Function name	Input type	Output type	Result type
GMCLIB_ElimDcBusRipFOC_F16	frac16_t	GMCLIB_2COOR_ALBE_T_F16 *	void
	GMCLIB_2COOR_ALBE_T_F16 *		
Compensation of a 16-bit fractional two-phase system input to a 16-bit fractional two-phase system, using a 16-bit fractional DC-bus voltage information. The DC-bus voltage input is within the fractional range $<0 ; 1$); the stationary (α - β) voltage input and the output are within the fractional range $<-1 ; 1$).			

NOTE

This algorithm can use the MMDVSQ peripheral module. See the following chapters for more details:

- [#unique_53](#) in Kinetis Design Studio
- [Memory-mapped divide and square root support](#) in Keil μ Vision
- [Memory-mapped divide and square root support](#) in IAR Embedded Workbench

2.7.2 Declaration

The available [GMCLIB_ElimDcBusRipFOC](#) functions have the following declarations:

```
void GMCLIB_ElimDcBusRipFOC_F16(frac16\_t f16UDcBus, const GMCLIB\_2COOR\_ALBE\_T\_F16 *psUAlBe,
GMCLIB\_2COOR\_ALBE\_T\_F16 *psUAlBeComp)
```

2.7.3 Function use

The use of the [GMCLIB_ElimDcBusRipFOC](#) function is shown in the following example:

```
#include "gmclib.h"

static frac16\_t f16UDcBus;
static GMCLIB\_2COOR\_ALBE\_T\_F16 sUAlBe;
static GMCLIB\_2COOR\_ALBE\_T\_F16 sUAlBeComp;

void Isr(void);

void main(void)
{
    /* Voltage Alpha, Beta structure initialization */
    sUAlBe.f16Alpha = FRAC16(0.0);
    sUAlBe.f16Beta = FRAC16(0.0);

    /* DC bus voltage initialization */
    f16UDcBus = FRAC16(0.8);
}

/* Periodical function or interrupt */
void Isr(void)
{
    /* FOC Ripple elimination calculation */
    GMCLIB_ElimDcBusRipFOC_F16(f16UDcBus, &sUAlBe, &sUAlBeComp);
}
```

2.8 GMCLIB_ElimDcBusRip

The [GMCLIB_ElimDcBusRip](#) function is used for a correct PWM duty cycle output calculation, based on the measured DC-bus voltage. The side effect is the elimination of the the DC-bus voltage ripple in the output PWM duty cycle. This function can be used with any kind of space vector modulation; it has an additional input - the modulation index (with respect to the DC-bus voltage).

The general equation to calculate the duty cycle is as follows:

$$U_{PWM} = \frac{u_{FOC}}{u_{dcbus}} \cdot i_{mod}$$

where:

- U_{PWM} is the duty cycle output
- u_{FOC} is the real FOC voltage
- u_{dcbus} is the real measured DC-bus voltage

- i_{mod} is the space vector modulation index

Using the previous equations, the [GMCLIB_ElimDcBusRip](#) function compensates an amplitude of the direct- α and the quadrature- β component of the stator-reference voltage vector, using the formula shown in the following equations:

$$U_{\alpha}^* = \begin{cases} 0, & U_{\alpha} = 0 \wedge U_{dcbus} = 0 \vee i_{mod} = 0 \\ 1, & U_{\alpha} > 0 \wedge |U_{\alpha}| \geq \frac{U_{dcbus}}{i_{mod}} \wedge i_{mod} > 0 \\ -1, & U_{\alpha} < 0 \wedge |U_{\alpha}| \geq \frac{U_{dcbus}}{i_{mod}} \wedge i_{mod} > 0 \\ \frac{U_{\alpha}}{U_{dcbus}} \cdot i_{mod}, & i_{mod} > 0 \end{cases}$$

$$U_{\beta}^* = \begin{cases} 0, & U_{\beta} = 0 \wedge U_{dcbus} = 0 \vee i_{mod} = 0 \\ 1, & U_{\beta} > 0 \wedge |U_{\beta}| \geq \frac{U_{dcbus}}{i_{mod}} \wedge i_{mod} > 0 \\ -1, & U_{\beta} < 0 \wedge |U_{\beta}| \geq \frac{U_{dcbus}}{i_{mod}} \wedge i_{mod} > 0 \\ \frac{U_{\beta}}{U_{dcbus}} \cdot i_{mod}, & i_{mod} > 0 \end{cases}$$

where:

- U_{α}^* is the direct- α duty cycle ratio
- U_{β}^* is the quadrature- β duty cycle ratio
- U_{α} is the direct- α voltage
- U_{β} is the quadrature- β voltage

If the fractional arithmetic is used, the FOC and DC-bus voltages have their scales, which take place in [GMCLIB_ElimDcBusRipFOC_Eq1](#); the equation is as follows:

$$U_{PWM} = \frac{U_{FOC} \cdot U_{FOC_max}}{U_{dcbus} \cdot U_{dcbus_max}} \cdot i_{mod} = \frac{U_{FOC}}{U_{dcbus}} \cdot \frac{U_{FOC_max}}{U_{dcbus_max}} \cdot i_{mod}$$

where:

- U_{FOC} is the scaled FOC voltage
- U_{dcbus} is the scaled measured DC-bus voltage
- U_{FOC_max} is the FOC voltage scale
- U_{dcbus_max} is the DC-bus voltage scale

Thus, the modulation index in the fractional representation is expressed as follows :

$$i_{modfr} = \frac{U_{FOC_max}}{U_{dcbus_max}} \cdot i_{mod}$$

where:

- i_{modfr} is the space vector modulation index in the fractional arithmetic

The [GMCLIB_ElimDcBusRip](#) function compensates an amplitude of the direct- α and the quadrature- β component of the stator-reference voltage vector in the fractional arithmetic, using the formula shown in the following equations:

$$U_{\alpha}^* = \begin{cases} 0, & U_{\alpha} = 0 \wedge U_{dcbus} = 0 \vee i_{modfr} = 0 \\ 1, & U_{\alpha} > 0 \wedge |U_{\alpha}| \geq \frac{U_{dcbus}}{i_{modfr}} \wedge i_{modfr} > 0 \\ -1, & U_{\alpha} < 0 \wedge |U_{\alpha}| \geq \frac{U_{dcbus}}{i_{modfr}} \wedge i_{modfr} > 0 \\ \frac{U_{\alpha}}{U_{dcbus}} \cdot i_{modfr}, & i_{modfr} > 0 \end{cases}$$

$$U_{\beta}^* = \begin{cases} 0, & U_{\beta} = 0 \wedge U_{dcbus} = 0 \vee i_{modfr} = 0 \\ 1, & U_{\beta} > 0 \wedge |U_{\beta}| \geq \frac{U_{dcbus}}{i_{modfr}} \wedge i_{modfr} > 0 \\ -1, & U_{\beta} < 0 \wedge |U_{\beta}| \geq \frac{U_{dcbus}}{i_{modfr}} \wedge i_{modfr} > 0 \\ \frac{U_{\beta}}{U_{dcbus}} \cdot i_{modfr}, & i_{modfr} > 0 \end{cases}$$

where:

- U_{α}^* is the direct- α duty cycle ratio
- U_{β}^* is the quadrature- β duty cycle ratio
- U_{α} is the direct- α voltage
- U_{β} is the quadrature- β voltage

The [GMCLIB_ElimDcBusRip](#) function can be used in general motor-control applications, and it provides elimination of the voltage ripple on the DC-bus of the power stage. [Figure 1](#) shows the results of the DC-bus ripple elimination, while compensating the ripples of the rectified voltage, using a three-phase uncontrolled rectifier.

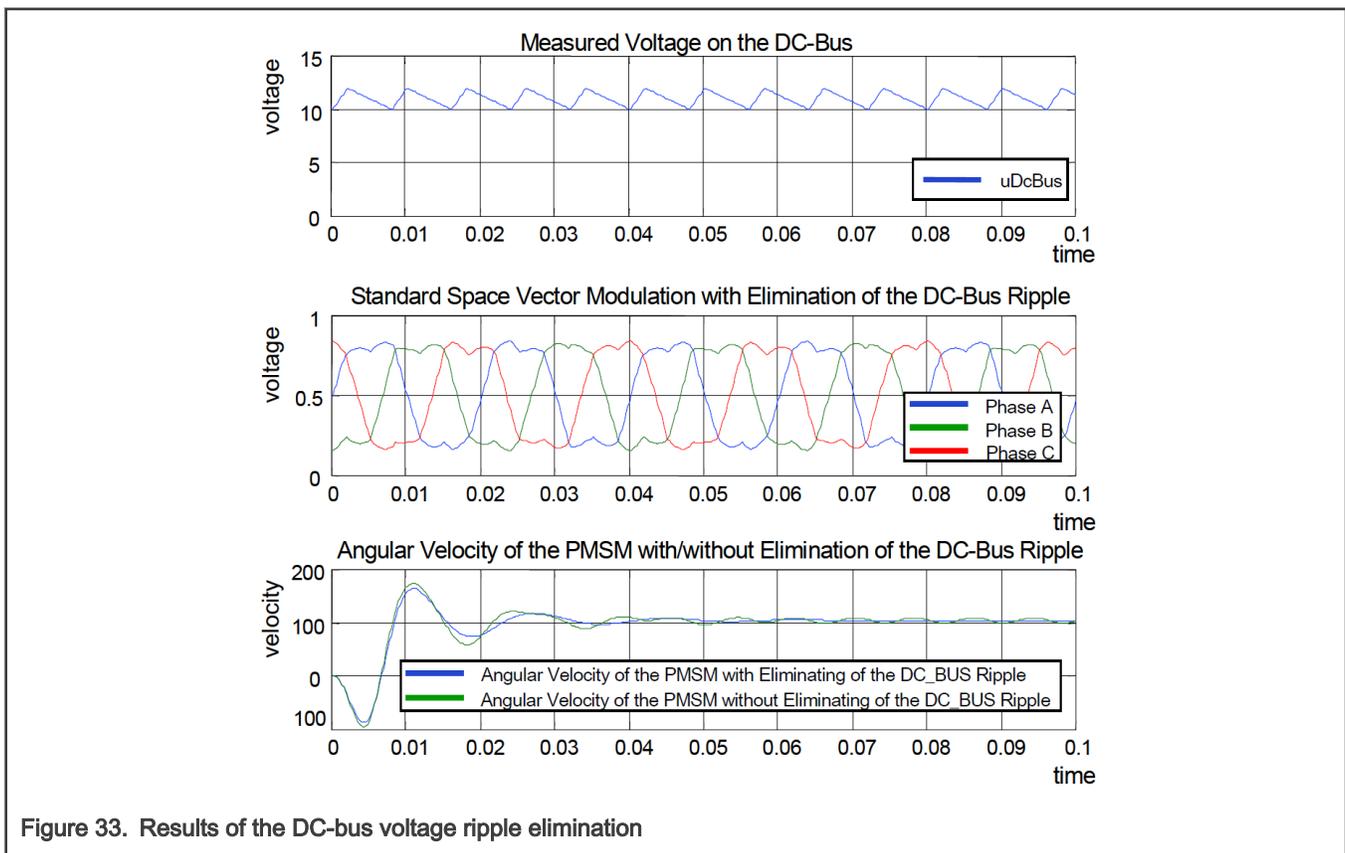


Figure 33. Results of the DC-bus voltage ripple elimination

2.8.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range $<-1 ; 1$). The result may saturate. The modulation index is a non-negative accumulator type value.

The available versions of the [GMCLIB_ElimDcBusRip](#) function are shown in the following table:

Table 9. Function versions

Function name	Input type	Output type	Result type
GMCLIB_ElimDcBusRip_F16sas	frac16_t	GMCLIB_2COOR_ALBE_T_F16 *	void
	acc32_t		
	GMCLIB_2COOR_ALBE_T_F16 *		
Compensation of a 16-bit fractional two-phase system input to a 16-bit fractional two-phase system using a 16-bit fractional DC-bus voltage information and a 32-bit accumulator modulation index. The DC-bus voltage input is within the fractional range $<0 ; 1$); the modulation index is a non-negative value; the stationary (α - β) voltage input and output are within the fractional range $<-1 ; 1$).			

NOTE

This algorithm can use the MMDVSQ peripheral module. See the following chapters for more details:

- [#unique_53](#) in Kinetis Design Studio
- [Memory-mapped divide and square root support](#) in Keil μ Vision
- [Memory-mapped divide and square root support](#) in IAR Embedded Workbench

2.8.2 Declaration

The available [GMCLIB_ElimDcBusRip](#) functions have the following declarations:

```
void GMCLIB_ElimDcBusRip_F16sas(frac16\_t f16UDcBus, acc32\_t a32IdxMod, const GMCLIB\_2COOR\_ALBE\_T\_F16
*psUAlBeComp, GMCLIB\_2COOR\_ALBE\_T\_F16 *psUAlBe)
```

2.8.3 Function use

The use of the [GMCLIB_ElimDcBusRip](#) function is shown in the following example:

```
#include "gmclib.h"

static frac16\_t f16UDcBus;
static acc32\_t a32IdxMod;
static GMCLIB\_2COOR\_ALBE\_T\_F16 sUAlBe;
static GMCLIB\_2COOR\_ALBE\_T\_F16 sUAlBeComp;

void Isr(void);

void main(void)
{
```

```
/* Voltage Alpha, Beta structure initialization */
sUAlBe.f16Alpha = FRAC16(0.0);
sUAlBe.f16Beta = FRAC16(0.0);

/* SVM modulation index */
a32IdxMod = ACC32(1.3);

/* DC bus voltage initialization */
f16UDcBus = FRAC16(0.8);
}

/* Periodical function or interrupt */
void Isr(void)
{
    /* Ripple elimination calculation */
    GMCLIB_ElimDcBusRip_F16sas(f16UDcBus, a32IdxMod, &sUAlBe, &sUAlBeComp);
}
```

2.9 GMCLIB_SvmStdShifted

The [GMCLIB_SvmStdShifted](#) function is based on the [GMCLIB_SvmStd](#) function and calculates the appropriate duty-cycle ratios, which are needed to generate the given stator-reference voltage vector using a special standard space-vector modulation technique. The [GMCLIB_SvmStdShifted](#) function enables the single-shunt measurement and current reconstruction and provides the data structures to configure the ADC and PWM peripherals.

The PWM signal generation by the [GMCLIB_SvmStdShifted](#) function applies a four-voltage vector in each PWM period:

- Two of them are inactive – vectors V0 (all switch elements are OFF – 000 states) and V7 (all switch elements are ON – 111 states).
- Two of them are active vectors that generate the motor power. See the table in [Figure 34](#).

Two phase currents are normally available as the DC-Bus current (i_{dcb}) during the active voltage vectors in each PWM period. It is possible to reconstruct all phase currents by measuring two different samples of i_{dcb} in each PWM period. The i_{dcb} current is 0 during V0 and V7. It can be used for offset measurement.

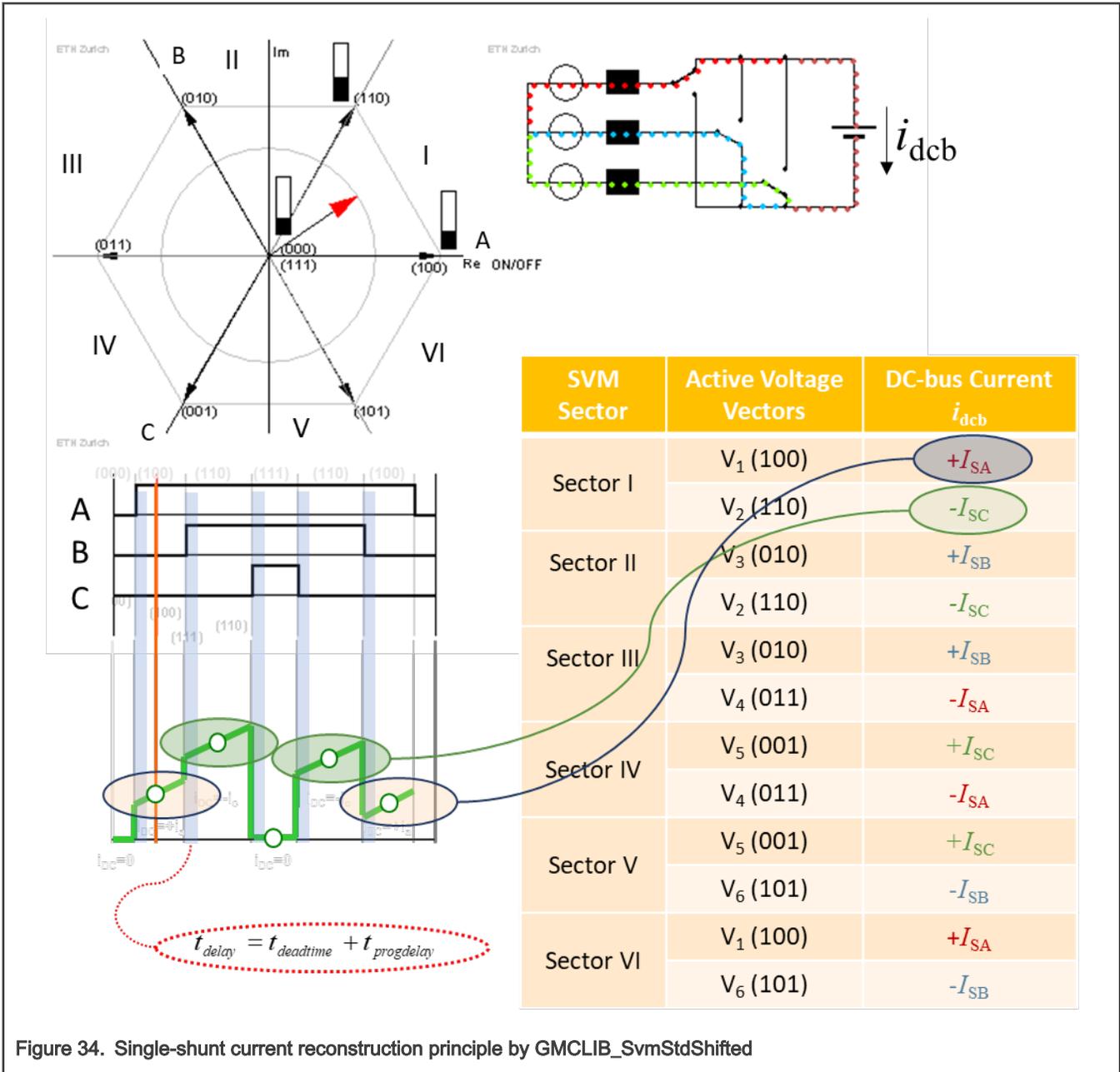


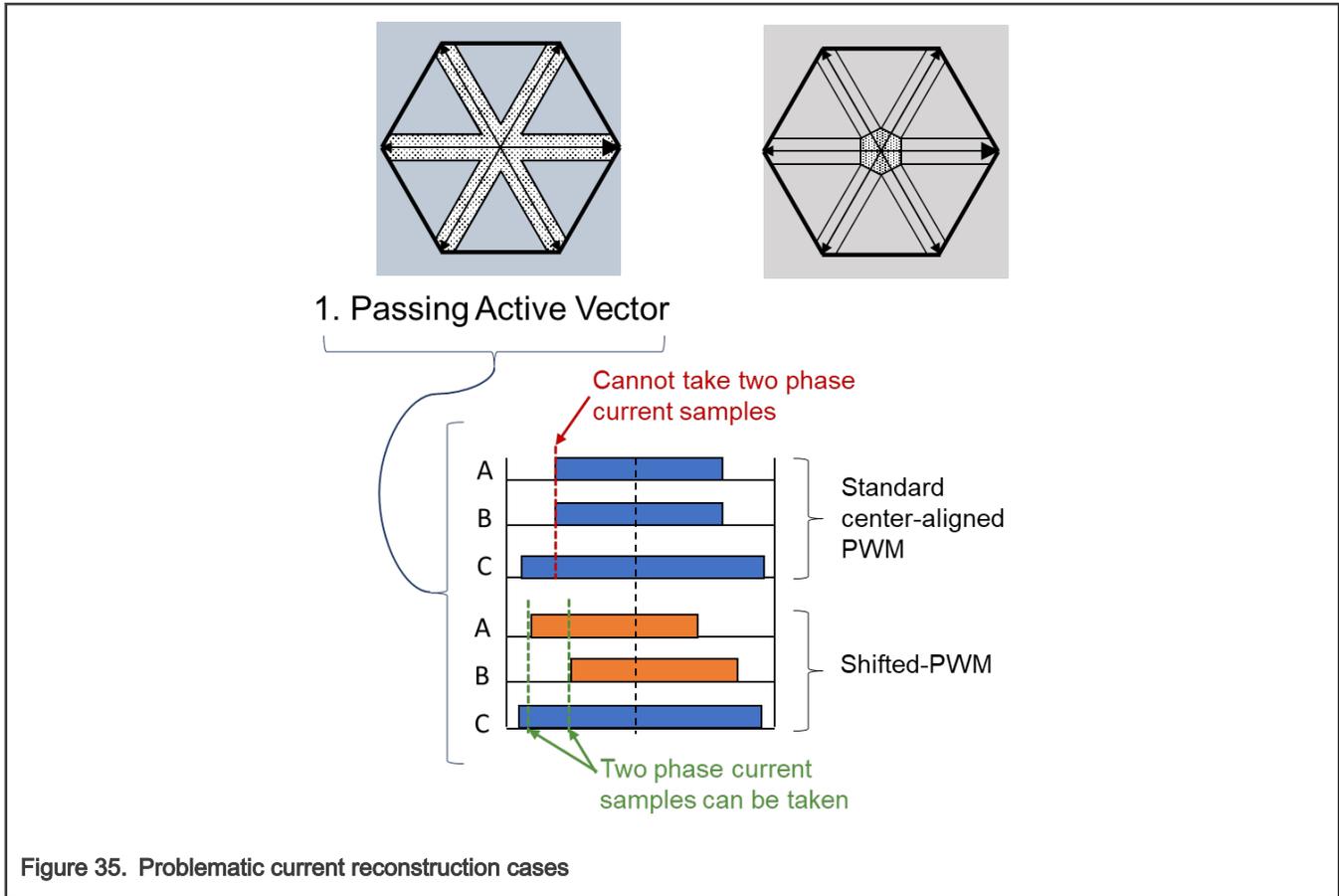
Figure 34. Single-shunt current reconstruction principle by GMCLIB_SvmStdShifted

Two different phase-current samples cannot be taken when:

- **The voltage vector is crossing the SVM sector border.** Only one sample can be taken.
- **The modulation index is low.** The sampling intervals are too short and no current samples can be taken.

There are many solutions available for these problems. For this function, the shifted-PWM method was used:

- The ON/OFF times are modified (shifted), if necessary.
- The duty cycles are preserved (the applied stator voltage is the same).



A different shifting strategy is applied for both critical cases:

1. Passing active vector:

- Freezes the center edge.
- Moves one critical edge.
- It is used for higher modulation indexes.

2. Low modulation indexes:

- Freezes the center edge.
- Moves both side edges in opposite directions.
- It is used for low modulation indexes.

The right method is selected within the SVM algorithm and shifts are applied by the PWM driver.

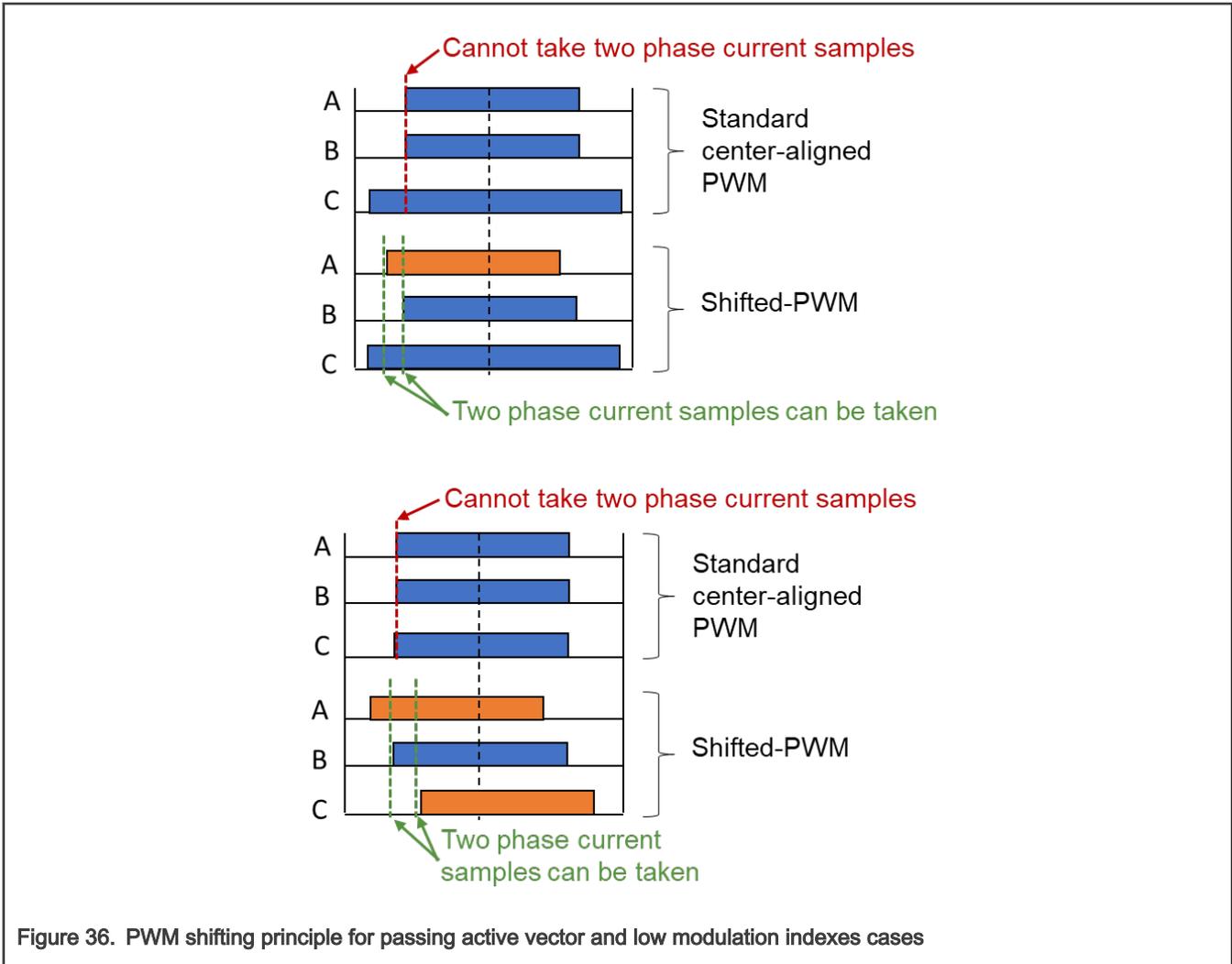


Figure 36. PWM shifting principle for passing active vector and low modulation indexes cases

2.9.1 Available versions

This function is available in the following versions:

- Fractional output - the duty-cycle outputs are the fractional portion of the result. The result is within the range of $<0 ; 1)$. The result may saturate.

Table 10. Function versions

Function name	Input/Output type		Result type
GMCLIB_SvmStdShiffted_F16	Inputs	GMCLIB_2COOR_ALBE_T_F16 *	void
	Parameter	GMCLIB_SVMSTDHIFTED_T_F16 *	
	Outputs	GMCLIB_ADC_CONFIG_T_F16 * , GMCLIB_PWM_CONFIG_T_F16 *	
Standard shifted space vector modulation with a 16-bit fractional stationary (α - β) input. The parameter is pointed to by an input pointer. The outputs are pointed to by output pointers. The result type is a void type.			

2.9.1.1 GMCLIB_SVMSTDSHIFTED_T_F16 type description

The input to configure the structure for the [GMCLIB_SvmStdShifted](#) function.

Variable name	Input type	Description
f16LowerLim	frac16_t	Low PWM duty-cycle limit. It influences any duty-cycle output in the sDuty structure of the PWM configuration structure. This parameter must be lower than f16UpperLim and of positive value within the range of <0 ; 1) as well. It is set by the user.
f16UpperLim	uint16_t	High PWM duty-cycle limit. It influences any duty-cycle output in the sDuty structure of the PWM configuration structure. This parameter must be higher than f16LowerLim and the value must be within the range of <0 ; 1) as well. It is set by the user.
f16MinT1T2	uint16_t	Minimum T1 or T2 time for a sufficient shift. It influences any shift output in the sShift structure of the PWM configuration structure. This parameter must be of a positive value and within the range of <0 ; 1). It is set by the user.

2.9.2 GMCLIB_ADC_CONFIG_T_F16 type description

The output structure to configure the ADC peripheral.

Variable name	Input type	Description
ui16SectorSVM	uint16_t	The output sector is an integer value within the range of <1 ; 6>. It is calculated by the algorithm and targeted to configure the ADC module.
f16SmplFirstEdge	frac16_t	The output delay for the first edge sample measurement. It is a 16-bit fractional value within the range of <-1 ; 1). It is calculated by the algorithm and targeted to configure the ADC module.
f16SmplSecondEdge	frac16_t	The output delay for the second sample measurement. It is a 16-bit fractional value within the range of <-1 ; 1). It is calculated by the algorithm and targeted to configure the ADC module.
eSmplOnePh	GMCLIB_PHASE_INDEX_T	The output value sets the first sample channel (phase) index. It is assigned from the algorithms and the enumeration value marks phase A, B, or C.
eSmplTwoPh	GMCLIB_PHASE_INDEX_T	The output value sets the second sample channel (phase) index. It is assigned from the algorithms and the enumeration value marks phase A, B, or C.
eCalcPh	GMCLIB_PHASE_INDEX_T	The output value sets the calculated sample channel (phase) index. It is assigned from the algorithms and the enumeration value marks phase A, B, or C.

2.9.3 GMCLIB_PWM_CONFIG_T_F16 type description

The output structure to configure the PWM peripheral.

Variable name		Input type	Description
sDuty	f16A	frac16_t	The phase-A duty cycle is a 16-bit fractional value within the range of <0 ; 1). It is calculated by the algorithms and targeted to configure the PWM module. It may be limited by upper or lower limits.
	f16B	frac16_t	The phase-B duty cycle is a 16-bit fractional value within the range of <0 ; 1). It is calculated by the algorithms and targeted to configure the PWM module. It may be limited by upper or lower limits.
	f16C	frac16_t	The phase-C duty cycle is a 16-bit fractional value within the range of <0 ; 1). It is calculated by the algorithms and targeted to configure the PWM module. It may be limited by upper or lower limits.
sShift	f16A	frac16_t	The phase-A shift is a 16-bit fractional value within the range of <-1 ; 1). It is calculated by the algorithms and targeted to configure the PWM module.
	f16B	frac16_t	The phase-B shift is a 16-bit fractional value within the range of <-1 ; 1). It is calculated by the algorithms and targeted to configure the PWM module.
	f16C	frac16_t	The phase-C shift is a 16-bit fractional value within the range of <-1 ; 1). It is calculated by the algorithms and targeted to configure the PWM module.

2.9.4 GMCLIB_PHASE_INDEX_T type description

The enum data type for labeling the phases in the [GMCLIB_ADC_CONFIG_T_F16](#) structure.

Name	Value	Description
kPhaseA	0U	Phase A
kPhaseB	1U	Phase B
kPhaseC	2U	Phase C

2.9.5 Declaration

The available [GMCLIB_SvmStdShifted](#) function has the following declaration:

```
void GMCLIB_SvmStdShifted_F16(const GMCLIB_2COOR_ALBE_T_F16 *psIn, const GMCLIB_SVMSTDSHIFTED_T_F16 *psParam, GMCLIB_ADC_CONFIG_T_F16 *psCfgMeas, GMCLIB_PWM_CONFIG_T_F16 *psCfgPWM)
```

2.9.6 Function use

The use of the [GMCLIB_SvmStdShifted](#) function is shown in the following example:

Fixed-point version:

```
#include "gmclib.h"

static GMCLIB_2COOR_ALBE_T_F16 sAlphaBetaIn;
static GMCLIB_SVMSTDSHIFTED_T_F16 sParam;
static GMCLIB_ADC_CONFIG_T_F16 sCfgMeas;
static GMCLIB_PWM_CONFIG_T_F16 sCfgPWM;

void Isr(void);
```

```

void main(void)
{
    /* Alpha, Beta voltage inputs */
    sAlphaBetaIn.fl6Alpha = FRAC16(0.25);
    sAlphaBetaIn.fl6Beta  = FRAC16(0.1)
    /* Set SvmStdShifted parameter */
    sParam.fl6LowerLim = FRAC16(0.01);
    sParam.fl6UpperLim = FRAC16(0.9);
    sParam.fl6MinT1T2  = FRAC16(0.1);
}
/* Periodical function or interrupt */
void Isr(void)
{
    /* SVM calculation update the output structures sCfgMeas and sCfPWM
    to configure the ADC and PWM modules */
    GMCLIB_SvmStdShifted_F16(&sAlphaBetaIn, &sParam, &sCfgMeas, &sCfPWM);
}
    
```

2.10 GMCLIB_SvmStd

The [GMCLIB_SvmStd](#) function calculates the appropriate duty-cycle ratios, which are needed for generation of the given stator-reference voltage vector, using a special standard space vector modulation technique.

The [GMCLIB_SvmStd](#) function for calculating the duty-cycle ratios is widely used in modern electric drives. This function calculates the appropriate duty-cycle ratios, which are needed for generating the given stator reference voltage vector, using a special space vector modulation technique, called standard space vector modulation.

The basic principle of the standard space vector modulation technique can be explained using the power stage diagram shown in [Figure 1](#).

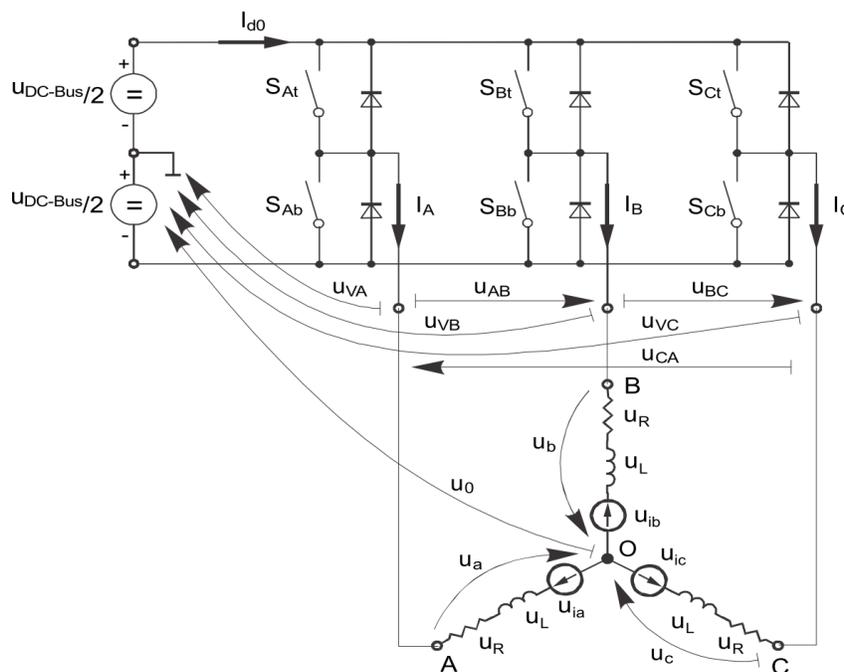


Figure 37. Power stage schematic diagram

The top and bottom switches are working in a complementary mode; for example, if the top switch S_{At} is on, then the corresponding bottom switch S_{Ab} is off, and vice versa. Considering that the value 1 is assigned to the ON state of the top switch, and value 0 is assigned to the ON state of the bottom switch, the switching vector $[a, b, c]^T$ can be defined. Creating of such vector allows for numerical definition of all possible switching states. Phase-to-phase voltages can then be expressed in terms of the following states:

$$\begin{bmatrix} U_{AB} \\ U_{BC} \\ U_{CA} \end{bmatrix} = U_{DCBus} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} a \\ b \\ c \end{bmatrix}$$

where U_{DCBus} is the instantaneous voltage measured on the DC-bus.

Assuming that the motor is completely symmetrical, it is possible to write a matrix equation, which expresses the motor phase voltages shown in [GMCLIB_SvmStd_Eq1](#).

$$\begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} = \frac{U_{DCBus}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \cdot \begin{bmatrix} a \\ b \\ c \end{bmatrix}$$

In a three-phase power stage configuration (as shown in [Figure 1](#)), eight possible switching states (shown in [Figure 2](#)) are feasible. These states, together with the resulting instantaneous output line-to-line and phase voltages, are listed in [Table 1](#).

Table 11. Switching patterns

A	B	C	U_a	U_b	U_c	U_{AB}	U_{BC}	U_{CA}	Vector
0	0	0	0	0	0	0	0	0	O_{000}
1	0	0	$2U_{DCBus}/3$	$-U_{DCBus}/3$	$-U_{DCBus}/3$	U_{DCBus}	0	$-U_{DCBus}$	U_0
1	1	0	$U_{DCBus}/3$	$U_{DCBus}/3$	$-2U_{DCBus}/3$	0	U_{DCBus}	$-U_{DCBus}$	U_{60}
0	1	0	$-U_{DCBus}/3$	$2U_{DCBus}/3$	$-U_{DCBus}/3$	$-U_{DCBus}$	U_{DCBus}	0	U_{120}
0	1	1	$-2U_{DCBus}/3$	$U_{DCBus}/3$	$U_{DCBus}/3$	$-U_{DCBus}$	0	U_{DCBus}	U_{240}
0	0	1	$-U_{DCBus}/3$	$-U_{DCBus}/3$	$2U_{DCBus}/3$	0	$-U_{DCBus}$	U_{DCBus}	U_{300}
1	0	1	$U_{DCBus}/3$	$-2U_{DCBus}/3$	$U_{DCBus}/3$	U_{DCBus}	$-U_{DCBus}$	0	U_{360}
1	1	1	0	0	0	0	0	0	O_{111}

The quantities of the direct- α and the quadrature- β components of the two-phase orthogonal coordinate system, describing the three-phase stator voltages, are expressed using the Clark transformation, arranged in a matrix form:

$$\begin{bmatrix} U_\alpha \\ U_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix}$$

The three-phase stator voltages - U_a , U_b , and U_c , are transformed using the Clark transformation into the direct- α and the quadrature- β components of the two-phase orthogonal coordinate system. The transformation results are listed in [Table 2](#).

Table 12. Switching patterns and space vectors

A	B	C	U_α	U_β	Vector
0	0	0	0	0	O_{000}
1	0	0	$2U_{DCBus}/3$	0	U_0

Table continues on the next page...

Table 12. Switching patterns and space vectors (continued)

A	B	C	U_α	U_β	Vector
1	1	0	$U_{DCBus}/3$	$U_{DCBus}/\sqrt{3}$	U_{60}
0	1	0	$-U_{DCBus}/3$	$U_{DCBus}/\sqrt{3}$	U_{120}
0	1	1	$-2U_{DCBus}/3$	0	U_{240}
0	0	1	$-U_{DCBus}/3$	$-U_{DCBus}/\sqrt{3}$	U_{300}
1	0	1	$U_{DCBus}/3$	$-U_{DCBus}/\sqrt{3}$	U_{360}
1	1	1	0	0	O_{111}

Figure 2 depicts the basic feasible switching states (vectors). There are six nonzero vectors - $U_0, U_{60}, U_{120}, U_{180}, U_{240}$, and U_{300} , and two zero vectors - O_{111} and O_{000} , usable for switching. Therefore, the principle of the standard space vector modulation lies in applying the appropriate switching states for a certain time, and thus generating a voltage vector identical to the reference one.

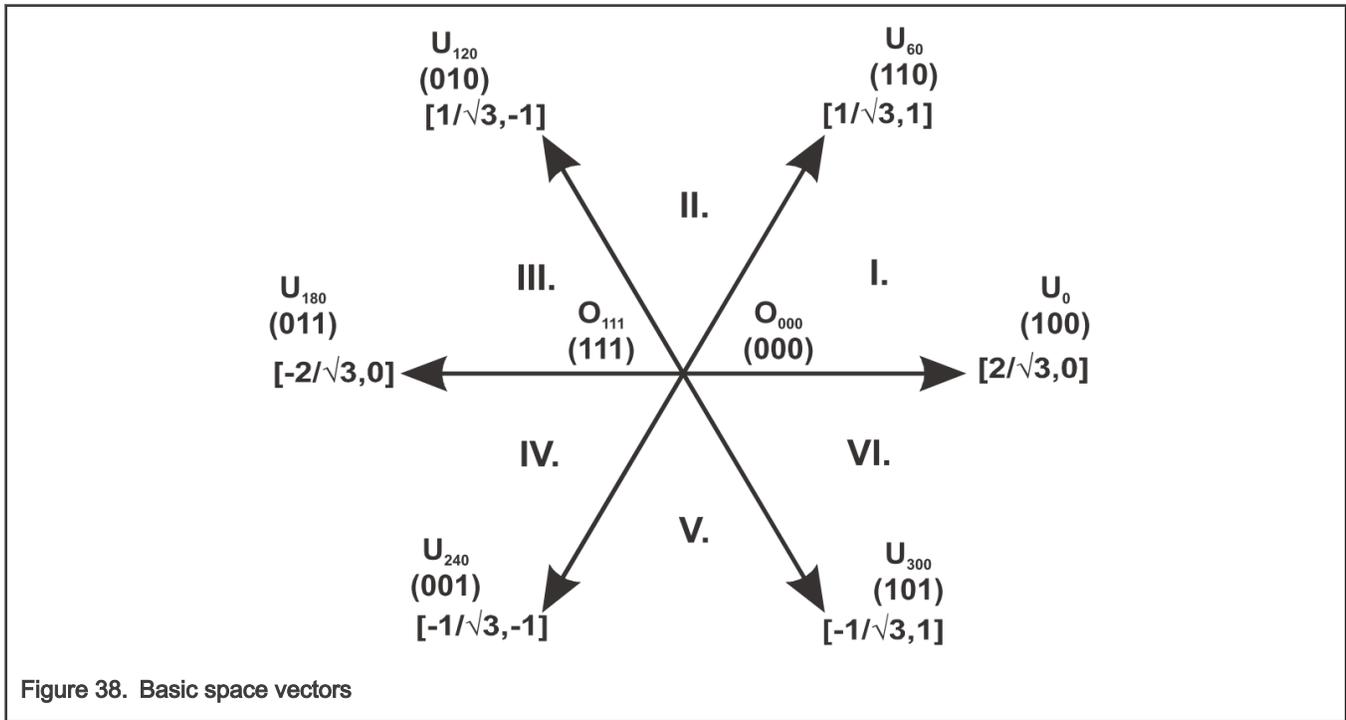


Figure 38. Basic space vectors

Referring to this principle, the objective of the standard space vector modulation is an approximation of the reference stator voltage vector U_S , with an appropriate combination of the switching patterns, composed of basic space vectors. The graphical explanation of this objective is shown in Figure 3 and Figure 4.

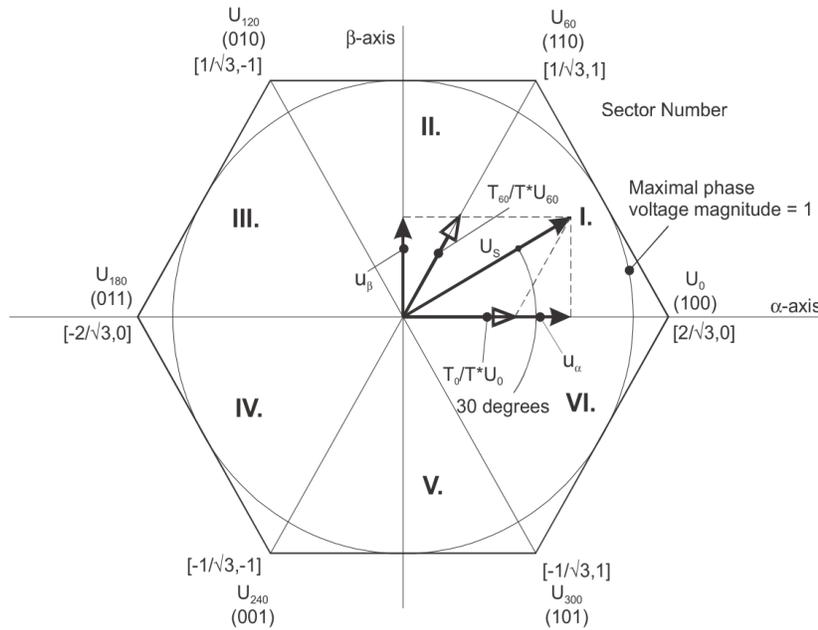


Figure 39. Projection of reference voltage vector in the respective sector

The stator reference voltage vector U_S is phase-advanced by 30° from the direct- α , and thus can be generated with an appropriate combination of the adjacent basic switching states U_0 and U_{60} . These figures also indicate the resultant direct- α and quadrature- β components for space vectors U_0 and U_{60} .

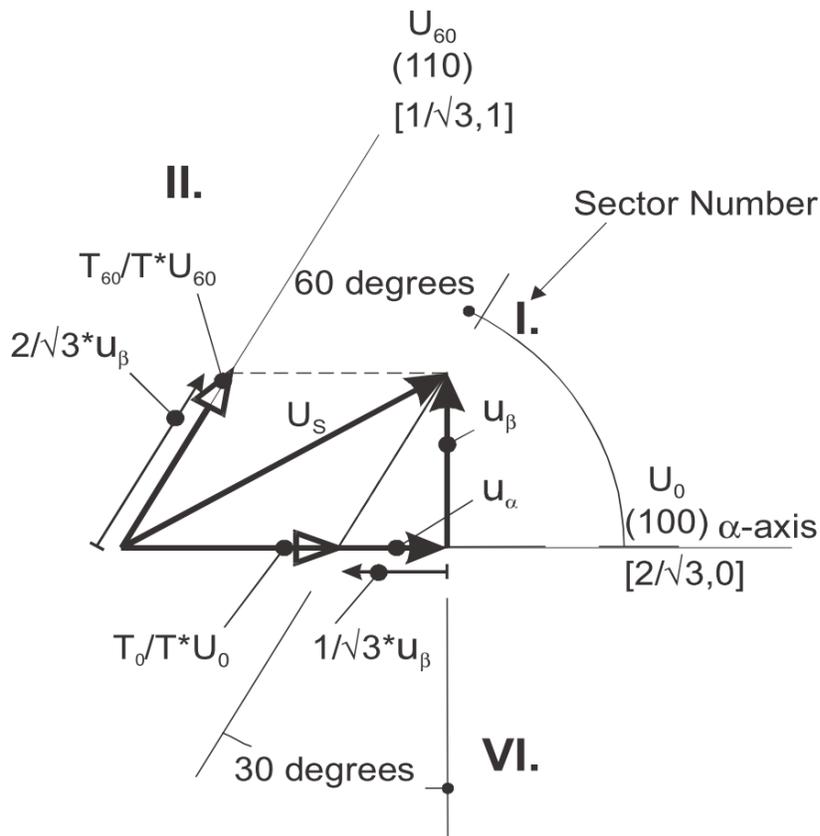


Figure 40. Detail of the voltage vector projection in the respective sector

In this case, the reference stator voltage vector U_S is located in sector I, and can be generated using the appropriate duty-cycle ratios of the basic switching states U_0 and U_{60} . The principal equations concerning this vector location are as follows:

$$T = T_{60} + T_0 + T_{null}$$

$$U_S = \frac{T_{60}}{T} \cdot U_{60} + \frac{T_0}{T} \cdot U_0$$

where T_{60} and T_0 are the respective duty-cycle ratios, for which the basic space vectors T_{60} and T_0 should be applied within the time period T . T_{null} is the time, for which the null vectors O_{000} and O_{111} are applied. Those duty-cycle ratios can be calculated using the following equations:

$$u_\beta = \frac{T_{60}}{T} \cdot |U_{60}| \cdot \sin 60^\circ$$

$$u_\alpha = \frac{T_0}{T} \cdot |U_0| + \frac{u_\beta}{\tan 60^\circ}$$

Considering that normalized magnitudes of basic space vectors are $|U_{60}| = |U_0| = 2/\sqrt{3}$, and by the substitution of the trigonometric expressions $\sin 60^\circ$ and $\tan 60^\circ$ by their quantities $2/\sqrt{3}$, and $\sqrt{3}$, respectively, the [GMCLIB_SvmStd_Eq5](#) can be rearranged for the unknown duty-cycle ratios T_{60}/T and T_0/T as follows:

$$\frac{T_{60}}{T} = u_\beta$$

$$U_S = \frac{T_{120}}{T} \cdot U_{120} + \frac{T_{60}}{T} \cdot U_{60}$$

Sector II is depicted in [GMCLIB_SvmStd_Img5](#). In this particular case, the reference stator voltage vector U_S is generated using the appropriate duty-cycle ratios of the basic switching states T_{60} and T_{120} . The basic equations describing this sector are as follows:

$$T = T_{120} + T_{60} + T_{null}$$

$$U_S = \frac{T_{120}}{T} \cdot U_{120} + \frac{T_{60}}{T} \cdot U_{60}$$

where T_{120} and T_{60} are the respective duty-cycle ratios, for which the basic space vectors U_{120} and U_{60} should be applied within the time period T . T_{null} is the time, for which the null vectors O_{000} and O_{111} are applied. These resultant duty-cycle ratios are formed from the auxiliary components, termed A and B. The graphical representation of the auxiliary components is shown in [GMCLIB_SvmStd_Img6](#).

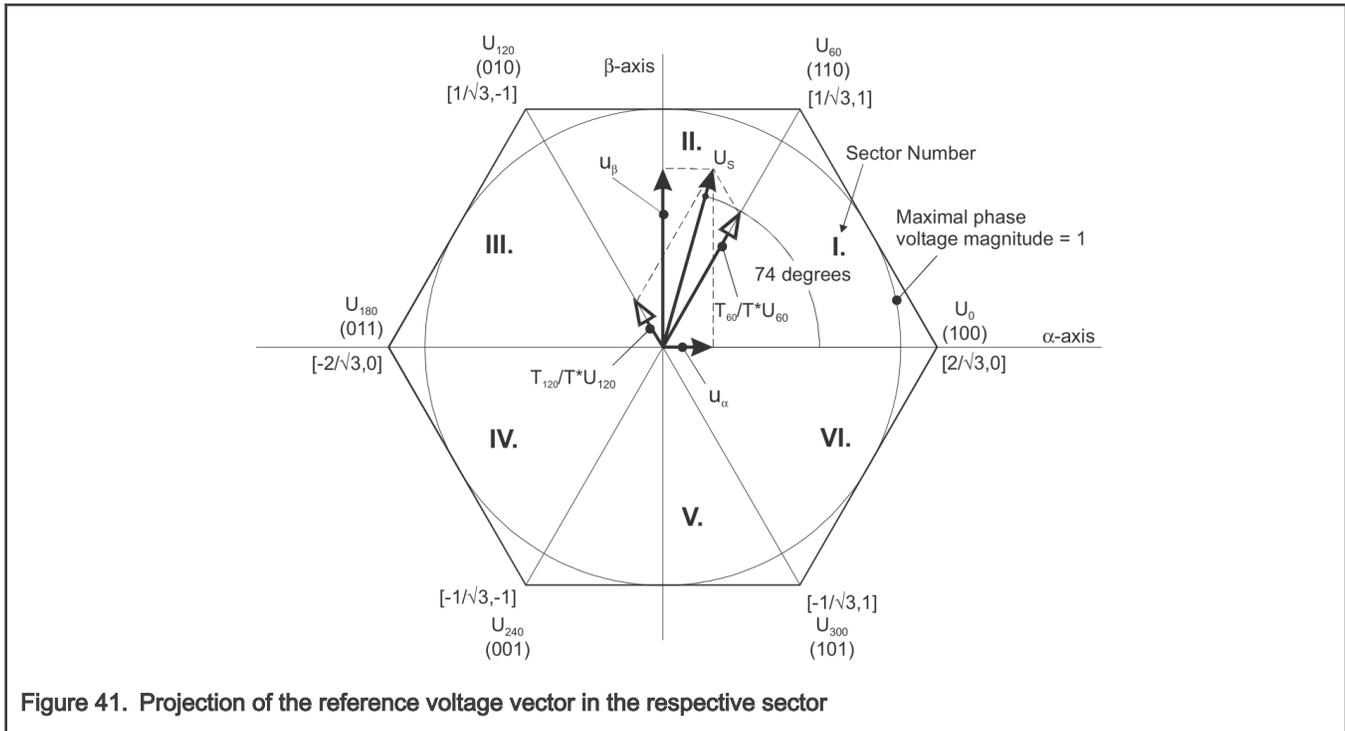


Figure 41. Projection of the reference voltage vector in the respective sector

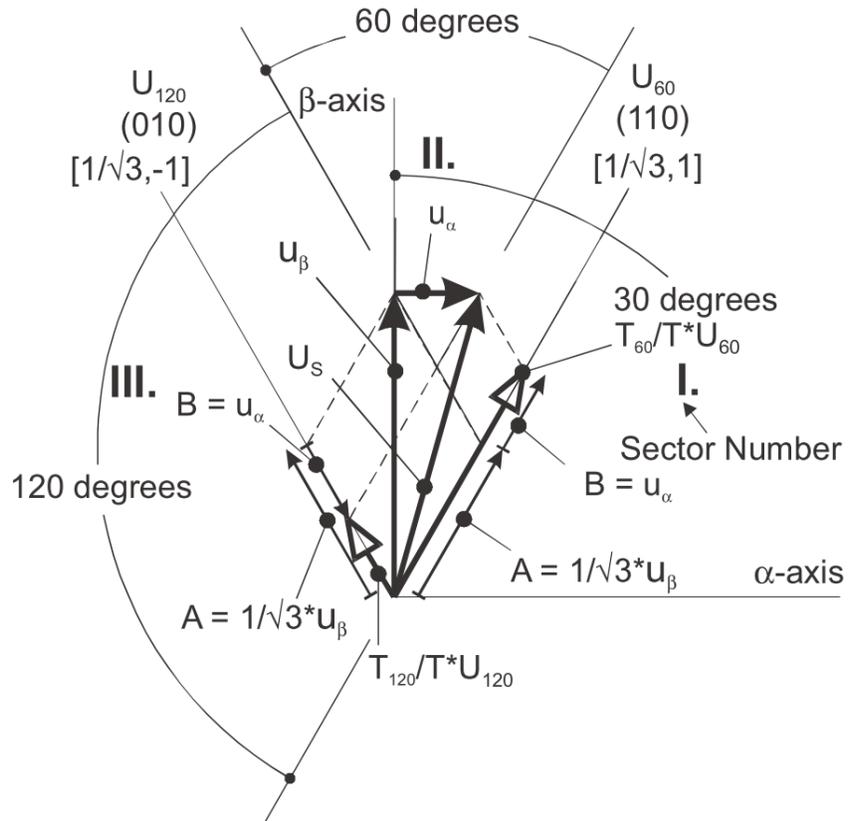


Figure 42. Detail of the voltage vector projection in the respective sector

The equations describing those auxiliary time-duration components are as follows:

$$\frac{\sin 30^\circ}{\sin 120^\circ} = \frac{A}{u_\beta}$$

$$\frac{\sin 60^\circ}{\sin 60^\circ} = \frac{B}{u_\alpha}$$

Equations in [GMCLIB_SvmStd_Eq8](#) have been created using the sine rule.

The resultant duty-cycle ratios T_{120} / T and T_{60} / T are then expressed in terms of the auxiliary time-duration components, defined by [GMCLIB_SvmStd_Eq9](#) as follows:

$$A = \frac{1}{\sqrt{3}} \cdot u_\beta$$

$$B = u_\alpha$$

Using these equations, and also considering that the normalized magnitudes of the basic space vectors are $|U_{120}| = |U_{60}| = 2 / \sqrt{3}$, the equations expressed for the unknown duty-cycle ratios of basic space vectors T_{120} / T and T_{60} / T can be expressed as follows:

$$\frac{T_{120}}{T} \cdot |U_{120}| = (A - B)$$

$$\frac{T_{60}}{T} \cdot |U_{60}| = (A + B)$$

The duty-cycle ratios in the remaining sectors can be derived using the same approach. The resulting equations will be similar to those derived for sector I and sector II.

$$\frac{T_{120}}{T} = \frac{1}{2}(u_{\beta} - \sqrt{3} \cdot u_{\alpha})$$

$$\frac{T_{60}}{T} = \frac{1}{2}(u_{\beta} + \sqrt{3} \cdot u_{\alpha})$$

To depict the duty-cycle ratios of the basic space vectors for all sectors, we define:

- Three auxiliary variables:

$$X = u_{\beta}$$

$$Y = \frac{1}{2}(u_{\beta} + \sqrt{3} \cdot u_{\alpha})$$

$$Z = \frac{1}{2}(u_{\beta} - \sqrt{3} \cdot u_{\alpha})$$

- Two expressions - $t_{_1}$ and $t_{_2}$, which generally represent the duty-cycle ratios of the basic space vectors in the respective sector (for example, for the first sector, $t_{_1}$ and $t_{_2}$), represent duty-cycle ratios of the basic space vectors U_{60} and U_0 ; for the second sector, $t_{_1}$ and $t_{_2}$ represent duty-cycle ratios of the basic space vectors U_{120} and U_{60} , and so on.

The expressions $t_{_1}$ and $t_{_2}$, in terms of auxiliary variables X, Y, and Z for each sector, are listed in [Table 3](#).

Table 13. Determination of $t_{_1}$ and $t_{_2}$ expressions

Sectors	U_0, U_{60}	U_{60}, U_{120}	U_{120}, U_{180}	U_{180}, U_{240}	U_{240}, U_{300}	U_{300}, U_0
$t_{_1}$	X	Y	-Y	Z	-Z	-X
$t_{_2}$	-Z	Z	X	-X	-Y	Y

For the determination of auxiliary variables X, Y, and Z, the sector number is required. This information can be obtained using several approaches. The approach discussed here requires the use of modified Inverse Clark transformation to transform the direct- α and quadrature- β components into balanced three-phase quantities u_{ref1} , u_{ref2} , and u_{ref3} , used for straightforward calculation of the sector number, to be shown later.

$$u_{ref1} = u_{\beta}$$

$$u_{ref2} = \frac{-u_{\beta} + \sqrt{3} \cdot u_{\alpha}}{2}$$

$$u_{ref3} = \frac{-u_{\beta} - \sqrt{3} \cdot u_{\alpha}}{2}$$

The modified Inverse Clark transformation projects the quadrature- u_{β} component into u_{ref1} , as shown in [GMCLIB_SvmStd_Img7](#) and [GMCLIB_SvmStd_Img8](#), whereas voltages generated by the conventional Inverse Clark transformation project the direct- u_{α} component into u_{ref1} .

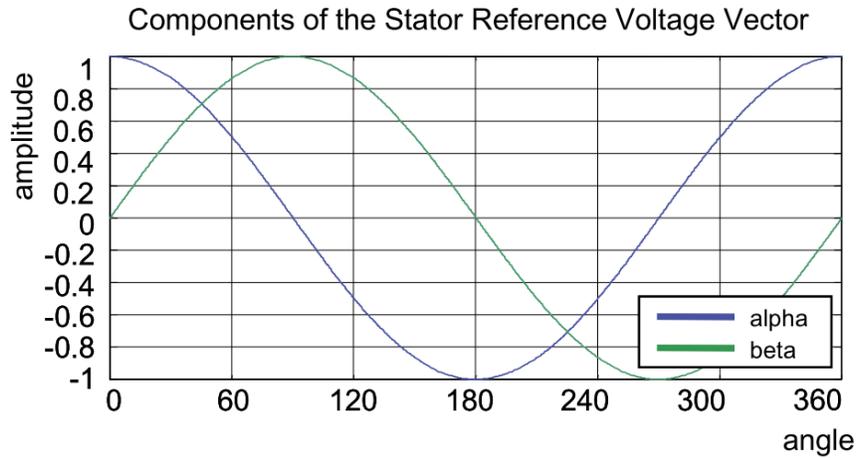


Figure 43. Direct- u_a and quadrature- u_b components of the stator reference voltage

GMCLIB_SvmStd_Img7 depicts the direct- u_a and quadrature- u_b components of the stator reference voltage vector U_S , which were calculated using equations $u_a = \cos \vartheta$ and $u_b = \sin \vartheta$, respectively.

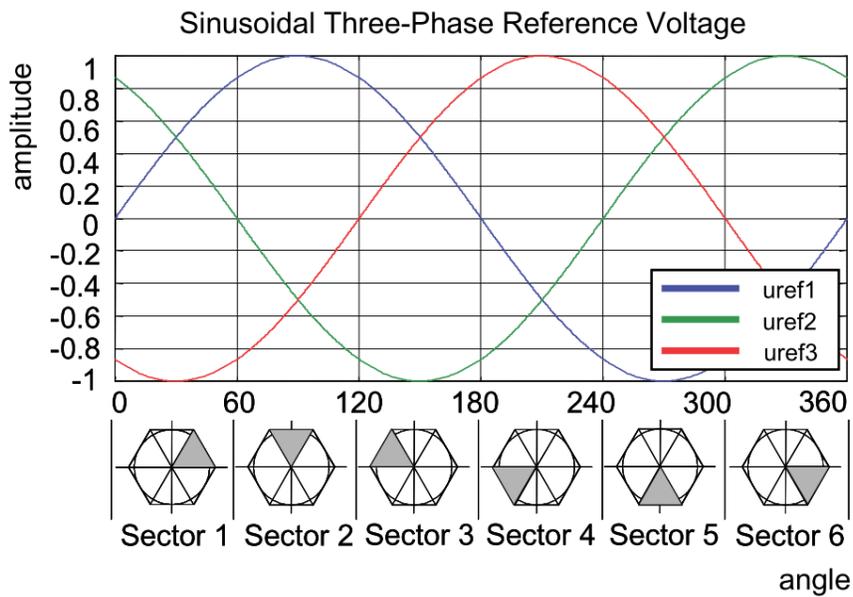
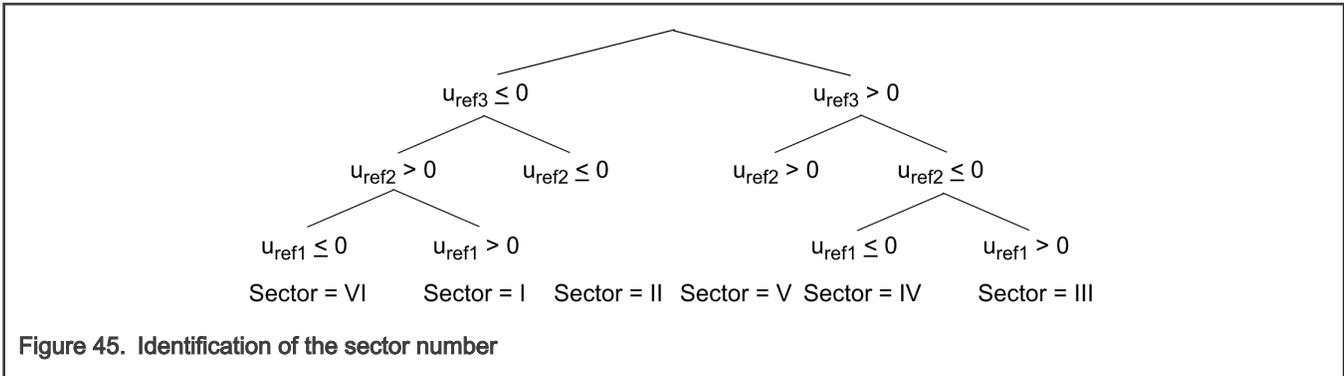


Figure 44. Reference voltages U_{ref1} , U_{ref2} , and U_{ref3}

The sector identification tree shown in GMCLIB_SvmStd_Img9 can be a numerical solution of the approach shown in GMCLIB_SvmStd_Img8.



In the worst case, at least three simple comparisons are required to precisely identify the sector of the stator reference voltage vector. For example, if the stator reference voltage vector is located as shown in [GMCLIB_SvmStd_Img3](#), the stator-reference voltage vector is phase-advanced by 30° from the direct α-axis, which results in the positive quantities of u_{ref1} and u_{ref2} , and the negative quantity of u_{ref3} ; see [GMCLIB_SvmStd_Img8](#). If these quantities are used as the inputs for the sector identification tree, the product of those comparisons will be sector I. The same approach identifies sector II, if the stator-reference voltage vector is located as shown in [GMCLIB_SvmStd_Img5](#). The variables t_1 , t_2 , and t_3 , which represent the switching duty-cycle ratios of the respective three-phase system, are calculated according to the following equations:

$$t_1 = \frac{T-t_{_1}t_{_2}}{2}$$

$$t_2 = t_1 + t_{_1}$$

$$t_3 = t_2 + t_{_2}$$

where T is the switching period, and $t_{_1}$ and $t_{_2}$ are the duty-cycle ratios of the basic space vectors given for the respective sector; [Table 3](#), [GMCLIB_SvmStd_Eq3](#), and [GMCLIB_SvmStd_Eq15](#) are specific solely to the standard space vector modulation technique; other space vector modulation techniques discussed later will require deriving different equations.

The next step is to assign the correct duty-cycle ratios - t_1 , t_2 , and t_3 , to the respective motor phases. This is a simple task, accomplished in a view of the position of the stator reference voltage vector; see .

Table 14. Assignment of the duty-cycle ratios to motor phases

Sectors	U_0, U_{60}	U_{60}, U_{120}	U_{120}, U_{180}	U_{180}, U_{240}	U_{240}, U_{300}	U_{300}, U_0
pwm_a	t_3	t_2	t_1	t_1	t_2	t_3
pwm_b	t_2	t_3	t_3	t_2	t_1	t_1
pwm_c	t_1	t_1	t_2	t_3	t_3	t_2

The principle of the space vector modulation technique consists of applying the basic voltage vectors U_{xxx} and O_{xxx} for certain time, in such a way that the main vector generated by the pulse width modulation approach for the period T is equal to the original stator reference voltage vector U_S . This provides a great variability of arrangement of the basic vectors during the PWM period T. These vectors might be arranged either to lower the switching losses, or to achieve diverse results, such as center-aligned PWM, edge-aligned PWM, or a minimal number of switching states. A brief discussion of the widely used center-aligned PWM follows.

Generating the center-aligned PWM pattern is accomplished by comparing the threshold levels pwm_a, pwm_b, and pwm_c with a free-running up-down counter. The timer counts to one, and then down to zero. It is supposed that when a threshold level is larger than the timer value, the respective PWM output is active. Otherwise, it is inactive; see [GMCLIB_SvmStd_Img10](#).

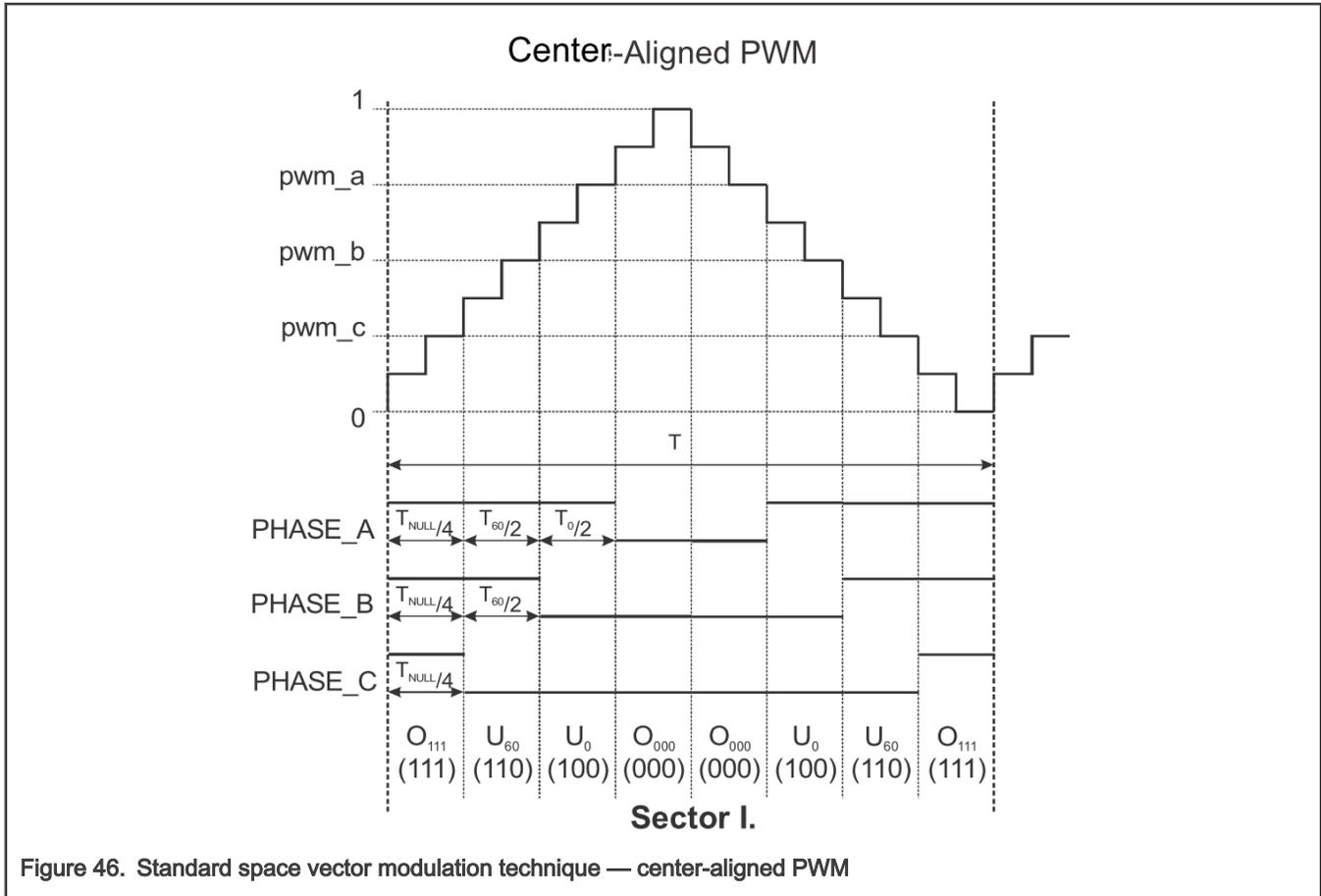


Figure 46. Standard space vector modulation technique — center-aligned PWM

GMCLIB_SvmStd_Img11 shows the waveforms of the duty-cycle ratios, calculated using standard space vector modulation.

For the accurate calculation of the duty-cycle ratios, direct- α , and quadrature- β components of the stator reference voltage vector, it must be considered that the duty cycle cannot be higher than one (100 %); in other words, the assumption

$$\sqrt{\alpha^2 + \beta^2} \leq 1$$

must be met.

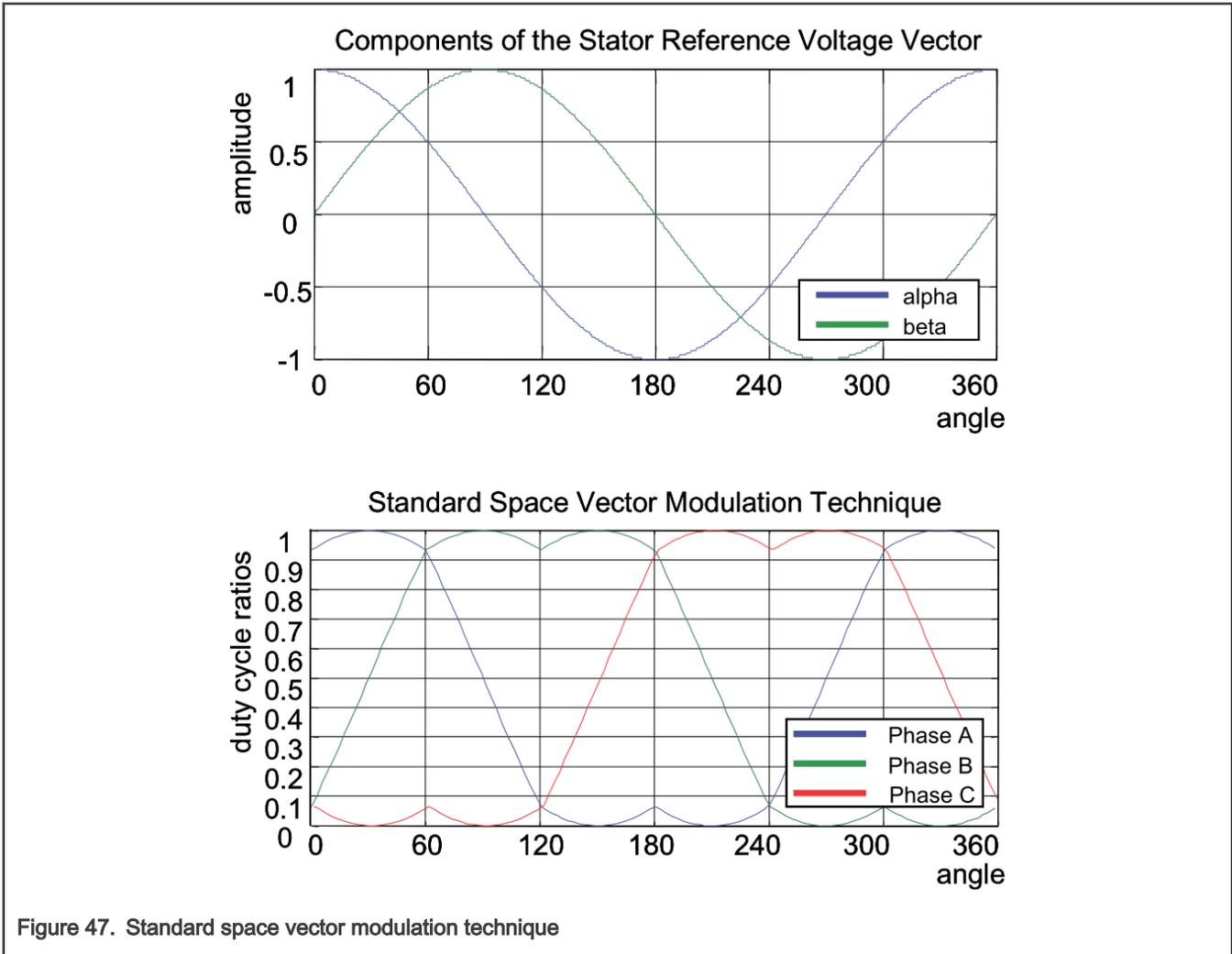


Figure 47. Standard space vector modulation technique

2.10.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range <0 ; 1). The result may saturate.

The available versions of the [GMCLIB_SvmStd](#) function are shown in the following table.

Table 15. Function versions

Function name	Input type	Output type	Result type
GMCLIB_SvmStd_F16	GMCLIB_2COOR_ALBE_T_F16 *	GMCLIB_3COOR_T_F16 *	uint16_t
	Standard space vector modulation with a 16-bit fractional stationary (α - β) input and a 16-bit fractional three-phase output. The result type is a 16-bit unsigned integer, which indicates the actual SVM sector. The input is within the range <-1 ; 1); the output duty cycle is within the range <0 ; 1). The output sector is an integer value within the range <1 ; 6>.		

2.10.2 Declaration

The available [GMCLIB_SvmStd](#) functions have the following declarations:

```
uint16_t GMCLIB_SvmStd_F16(const GMCLIB\_2COOR\_ALBE\_T\_F16 *psIn, GMCLIB\_3COOR\_T\_F16 *psOut)
```

2.10.3 Function use

The use of the `GMCLIB_SvmStd` function is shown in the following example:

```
#include "gmclib.h"

static uint16_t u16Sector;
static GMCLIB_2COOR_ALBE_T_F16 sAlphaBeta;
static GMCLIB_3COOR_T_F16 sAbc;

void Isr(void);

void main(void)
{
    /* Alpha, Beta structure initialization */
    sAlphaBeta.f16Alpha = FRAC16(0.0);
    sAlphaBeta.f16Beta = FRAC16(0.0);
}

/* Periodical function or interrupt */
void Isr(void)
{
    /* SVM calculation */
    u16Sector = GMCLIB_SvmStd_F16(&sAlphaBeta, &sAbc);
}
```

2.11 GMCLIB_SvmIct

The `GMCLIB_SvmIct` function calculates the appropriate duty-cycle ratios, which are needed for generation of the given stator-reference voltage vector using the general sinusoidal modulation technique.

The `GMCLIB_SvmIct` function calculates the appropriate duty-cycle ratios, needed for generation of the given stator reference voltage vector using the conventional Inverse Clark transformation. Finding the sector in which the reference stator voltage vector U_S resides is similar to `GMCLIB_SvmStd`. This is achieved by first converting the direct- α and the quadrature- β components of the reference stator voltage vector U_S into the balanced three-phase quantities u_{ref1} , u_{ref2} , and u_{ref3} using the modified Inverse Clark transformation:

$$\begin{aligned} u_{ref1} &= u_\beta \\ u_{ref2} &= \frac{-u_\beta + \sqrt{3}u_\alpha}{2} \\ u_{ref3} &= \frac{-u_\beta - \sqrt{3}u_\alpha}{2} \end{aligned}$$

The calculation of the sector number is based on comparing the three-phase reference voltages u_{ref1} , u_{ref2} , and u_{ref3} with zero. This computation is described by the following set of rules:

$$\begin{aligned} a &= \begin{cases} 1, & u_{ref1} > 0 \\ 0, & \text{else} \end{cases} \\ b &= \begin{cases} 2, & u_{ref2} > 0 \\ 0, & \text{else} \end{cases} \\ c &= \begin{cases} 4, & u_{ref3} > 0 \\ 0, & \text{else} \end{cases} \end{aligned}$$

After passing these rules, the modified sector numbers are then derived using the following formula:

$$sector^* = a + b + c$$

The sector numbers determined by this formula must be further transformed to correspond to those determined by the sector identification tree. The transformation which meets this requirement is shown in the following table:

Table 16. Transformation of the sectors

Sector*	1	2	3	4	5	6
Sector	2	6	1	4	3	5

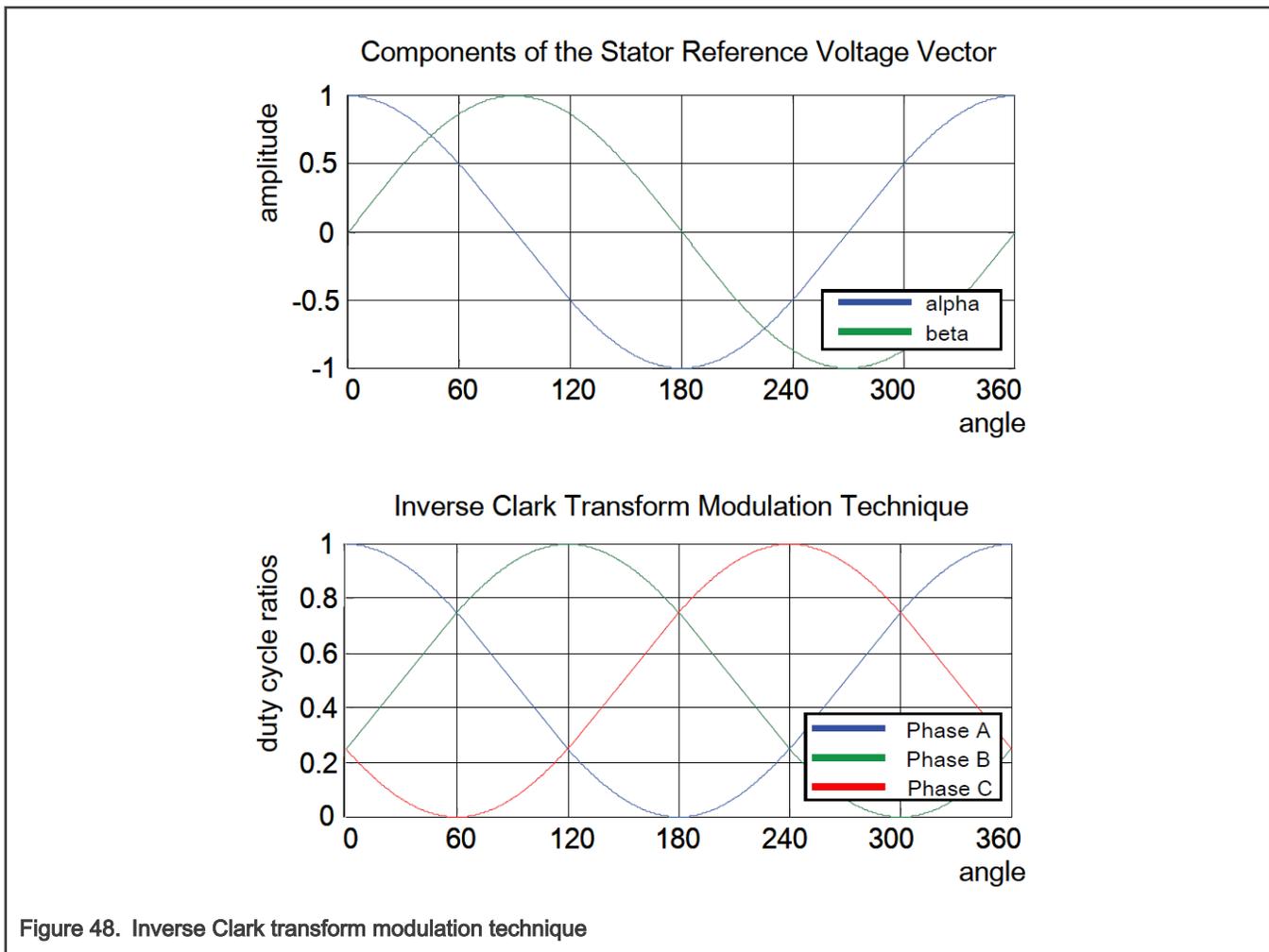
Use the Inverse Clark transformation for transforming values such as flux, voltage, and current from an orthogonal rotating coordination system (u_α, u_β) to a three-phase rotating coordination system ($u_a, u_b,$ and u_c). The original equations of the Inverse Clark transformation are scaled here to provide the duty-cycle ratios in the range $<0 ; 1$). These scaled duty cycle ratios $pwm_a,$ $pwm_b,$ and pwm_c can be used directly by the registers of the PWM block.

$$pwm_a = 0.5 + \frac{u_\alpha}{2}$$

$$pwm_b = 0.5 + \frac{-u_\alpha + \sqrt{3}u_\beta}{4}$$

$$pwm_c = 0.5 + \frac{-u_\alpha - \sqrt{3}u_\beta}{4}$$

The following figure shows the waveforms of the duty-cycle ratios calculated using the Inverse Clark transformation.



For an accurate calculation of the duty-cycle ratios and the direct- α and quadrature- β components of the stator reference voltage vector, the duty cycle cannot be higher than one (100 %); in other words, the assumption

$$\sqrt{\alpha^2 + \beta^2} \leq 1$$

must be met.

2.11.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range $\langle 0 ; 1 \rangle$. The result may saturate.

The available versions of the [GMCLIB_SvmIct](#) function are shown in the following table:

Table 17. Function versions

Function name	Input type	Output type	Result type
GMCLIB_SvmIct_F16	GMCLIB_2COOR_ALBE_T_F16 *	GMCLIB_3COOR_T_F16 *	uint16_t
	General sinusoidal space vector modulation with a 16-bit fractional stationary (α - β) input and a 16-bit fractional three-phase output. The result type is a 16-bit unsigned integer, which indicates the actual SVM sector. The input is within the range $\langle -1 ; 1 \rangle$; the output duty cycle is within the range $\langle 0 ; 1 \rangle$. The output sector is an integer value within the range $\langle 1 ; 6 \rangle$.		

2.11.2 Declaration

The available [GMCLIB_SvmIct](#) functions have the following declarations:

```
uint16_t GMCLIB_SvmIct_F16(const GMCLIB\_2COOR\_ALBE\_T\_F16 *psIn, GMCLIB\_3COOR\_T\_F16 *psOut)
```

2.11.3 Function use

The use of the [GMCLIB_SvmIct](#) function is shown in the following example:

```
#include "gmclib.h"

static uint16_t ul6Sector;
static GMCLIB\_2COOR\_ALBE\_T\_F16 sAlphaBeta;
static GMCLIB\_3COOR\_T\_F16 sAbc;

void Isr(void);

void main(void)
{
    /* Alpha, Beta structure initialization */
    sAlphaBeta.f16Alpha = FRAC16(0.0);
    sAlphaBeta.f16Beta = FRAC16(0.0);
}

/* Periodical function or interrupt */
void Isr(void)
{
    /* SVM calculation */
    ul6Sector = GMCLIB_SvmIct_F16(&sAlphaBeta, &sAbc);
}
```

2.12 GMCLIB_SvmU0n

The [GMCLIB_SvmU0n](#) function calculates the appropriate duty-cycle ratios, which are needed for generation of the given stator-reference voltage vector using the general sinusoidal modulation technique.

The [GMCLIB_SvmU0n](#) function for calculating of duty-cycle ratios is widely used in modern electric drives. This function calculates the appropriate duty-cycle ratios, which are needed for generating the given stator reference voltage vector using a special space vector modulation technique called space vector modulation with O_{000} nulls, where only one type of null vector O_{000} is used (all bottom switches are turned on in the inverter).

The derivation approach of the space vector modulation technique with O_{000} nulls is in many aspects identical to the approach presented in [GMCLIB_SvmStd](#). However, a distinct difference lies in the definition of the variables t_1 , t_2 , and t_3 that represent switching duty-cycle ratios of the respective phases:

$$\begin{aligned}
 t_1 &= 0 \\
 t_2 &= t_1 + t_{_1} \\
 t_3 &= t_2 + t_{_2}
 \end{aligned}$$

where T is the switching period, and $t_{_1}$ and $t_{_2}$ are the duty-cycle ratios of the basic space vectors that are defined for the respective sector in [Table 2-7](#).

The generally used center-aligned PWM is discussed briefly in the following sections. Generating the center-aligned PWM pattern is accomplished practically by comparing the threshold levels pwm_a , pwm_b , and pwm_c with the free-running up/down counter. The timer counts up to 1 (0x7FFF) and then down to 0 (0x0000). It is supposed that when a threshold level is larger than the timer value, the respective PWM output is active. Otherwise it is inactive (see [GMCLIB_SvmU0n_Img1](#)).

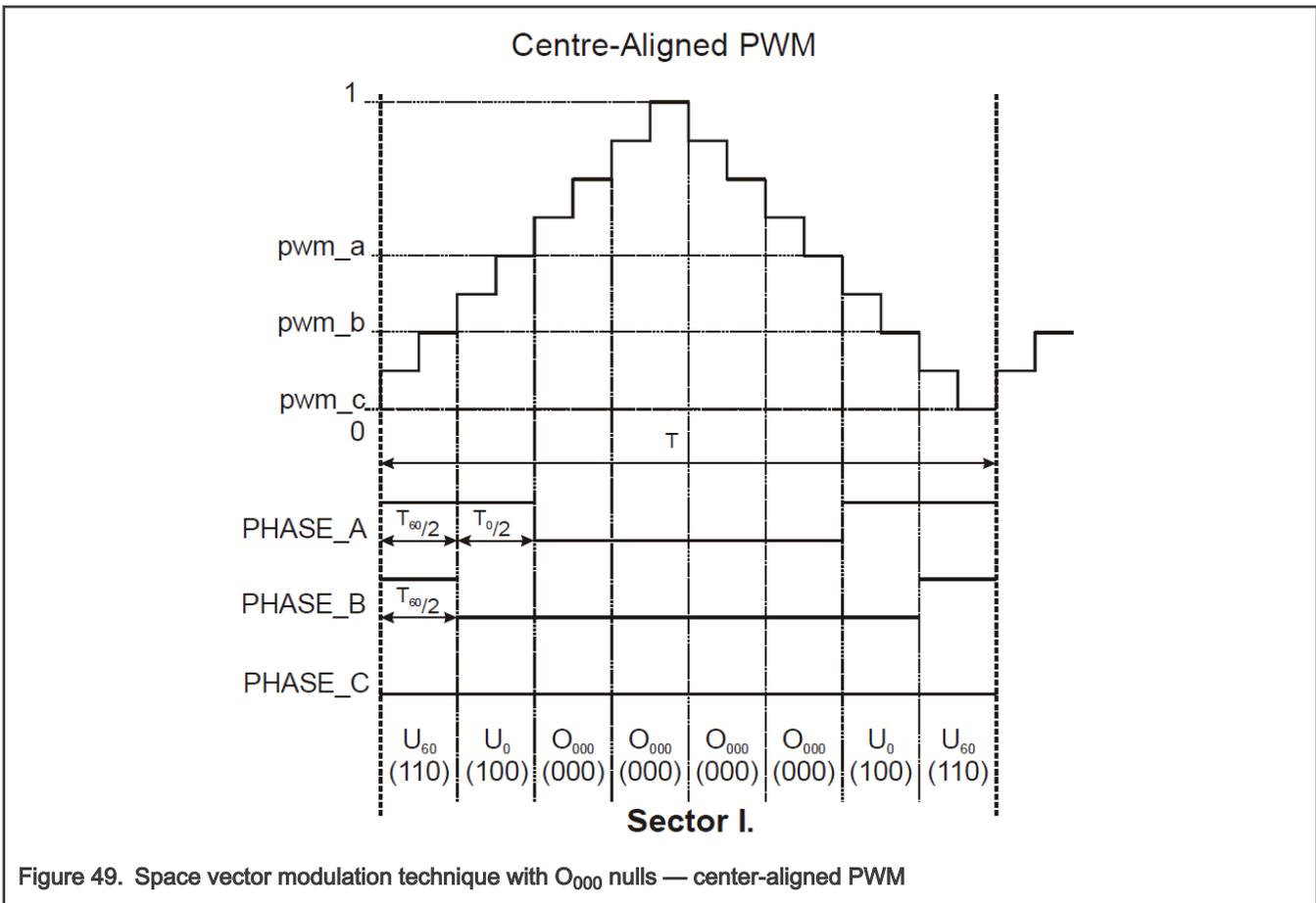


Figure 49. Space vector modulation technique with O_{000} nulls — center-aligned PWM

Figure [GMCLIB_SvmU0n_Img1](#) shows calculated waveforms of the duty cycle ratios using space vector modulation with O_{000} nulls.

For an accurate calculation of the duty-cycle ratios, direct- α , and quadrature- β components of the stator reference voltage vector, consider that the duty cycle cannot be higher than one (100 %); in other words, the assumption

$$\sqrt{\alpha^2 + \beta^2} \leq 1$$

must be met.

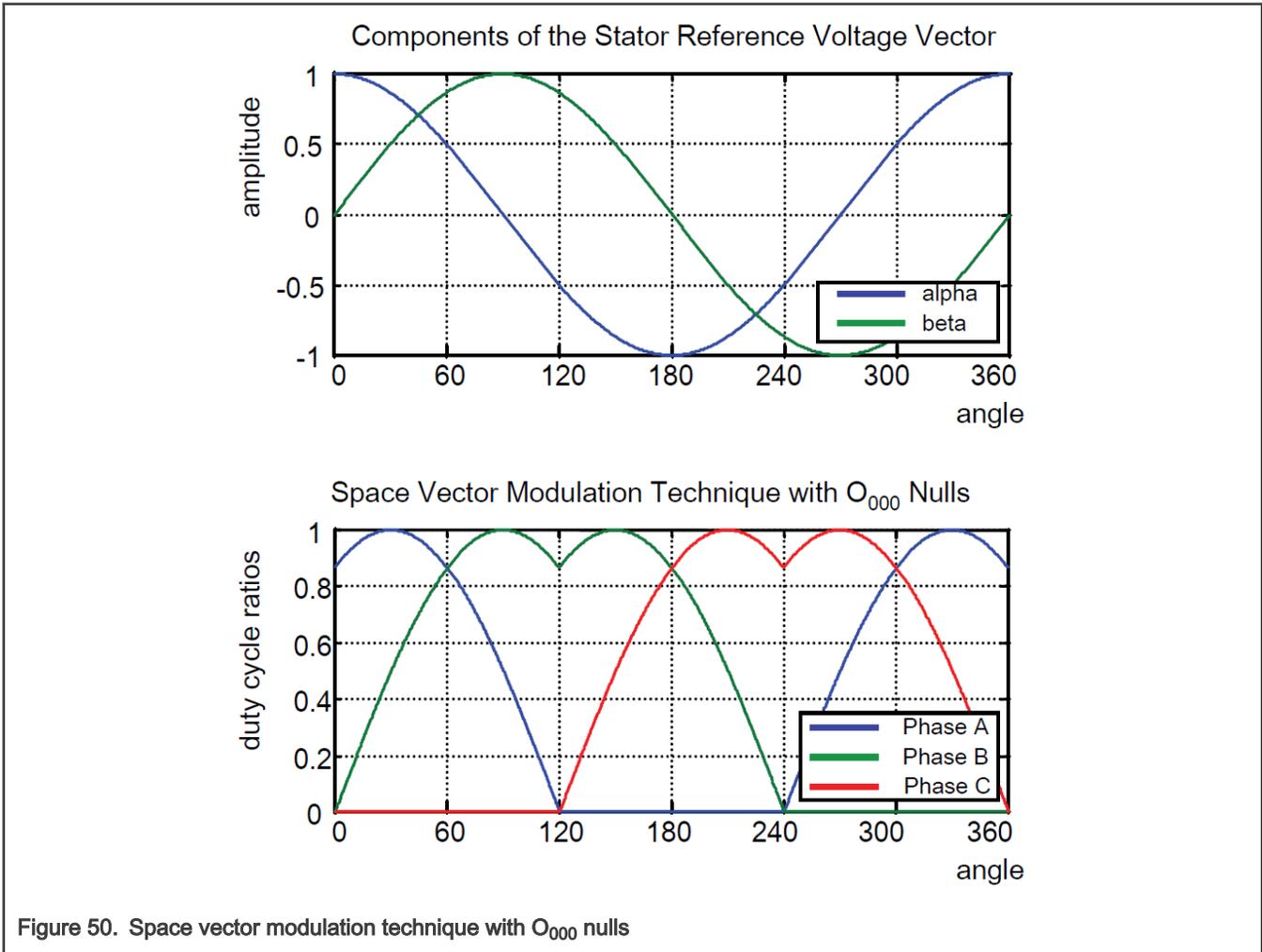


Figure 50. Space vector modulation technique with O_{000} nulls

2.12.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range $<0 ; 1$). The result may saturate.

The available versions of the [GMCLIB_SvmU0n](#) function are shown in the following table:

Table 18. Function versions

Function name	Input type	Output type	Result type
GMCLIB_SvmU0n_F16	GMCLIB_2COOR_ALBE_T_F16 *	GMCLIB_3COOR_T_F16 *	uint16_t
	General sinusoidal space vector modulation with a 16-bit fractional stationary (α - β) input, and a 16-bit fractional three-phase output. The result type is a 16-bit unsigned integer, which indicates the actual		

Table continues on the next page...

Table 18. Function versions

Function name	Input type	Output type	Result type
	SVM sector. The input is within the range <-1 ; 1); the output duty cycle is within the range <0 ; 1). The output sector is an integer value within the range <1 ; 6>.		

2.12.2 Declaration

The available [GMCLIB_SvmU0n](#) functions have the following declarations:

```
uint16_t GMCLIB_SvmU0n_F16(const GMCLIB_2COOR_ALBE_T_F16 *psIn, GMCLIB_3COOR_T_F16 *psOut)
```

2.12.3 Function use

The use of the [GMCLIB_SvmU0n](#) function is shown in the following example:

```
#include "gmclib.h"

static uint16_t ul6Sector;
static GMCLIB_2COOR_ALBE_T_F16 sAlphaBeta;
static GMCLIB_3COOR_T_F16 sAbc;

void Isr(void);

void main(void)
{
    /* Alpha, Beta structure initialization */
    sAlphaBeta.f16Alpha = FRAC16(0.0);
    sAlphaBeta.f16Beta = FRAC16(0.0);
}

/* Periodical function or interrupt */
void Isr(void)
{
    /* SVM calculation */
    ul6Sector = GMCLIB_SvmU0n_F16(&sAlphaBeta, &sAbc);
}
```

2.13 GMCLIB_SvmU7n

The [GMCLIB_SvmU7n](#) function calculates the appropriate duty-cycle ratios, which are needed for generation of the given stator-reference voltage vector, using the general sinusoidal modulation technique.

The [GMCLIB_SvmU7n](#) function for calculating the duty-cycle ratios is widely used in modern electric drives. This function calculates the appropriate duty-cycle ratios, which are needed for generating the given stator reference voltage vector using a special space vector modulation technique called space vector modulation with O_{111} nulls, where only one type of null vector O_{111} is used (all top switches are turned on in the inverter).

The derivation approach of the space vector modulation technique with O_{111} nulls is identical (in many aspects) to the approach presented in [GMCLIB_SvmStd](#). However, a distinct difference lies in the definition of variables t_1 , t_2 , and t_3 that represent switching duty-cycle ratios of the respective phases:

$$\begin{aligned}
 t_1 &= T - t_{-1} - t_{-2} \\
 t_2 &= t_1 + t_{-1} \\
 t_3 &= t_2 + t_{-2}
 \end{aligned}$$

where T is the switching period, and t₋₁ and t₋₂ are the duty-cycle ratios of the basic space vectors defined for the respective sector in [Table 2-7](#).

The generally-used center-aligned PWM is discussed briefly in the following sections. Generating the center-aligned PWM pattern is accomplished by comparing threshold levels pwm_a, pwm_b, and pwm_c with the free-running up/down counter. The timer counts up to 1 (0x7FFF) and then down to 0 (0x0000). It is supposed that when a threshold level is larger than the timer value, the respective PWM output is active. Otherwise, it is inactive (see [GMCLIB_SvmU7n_Img1](#)).

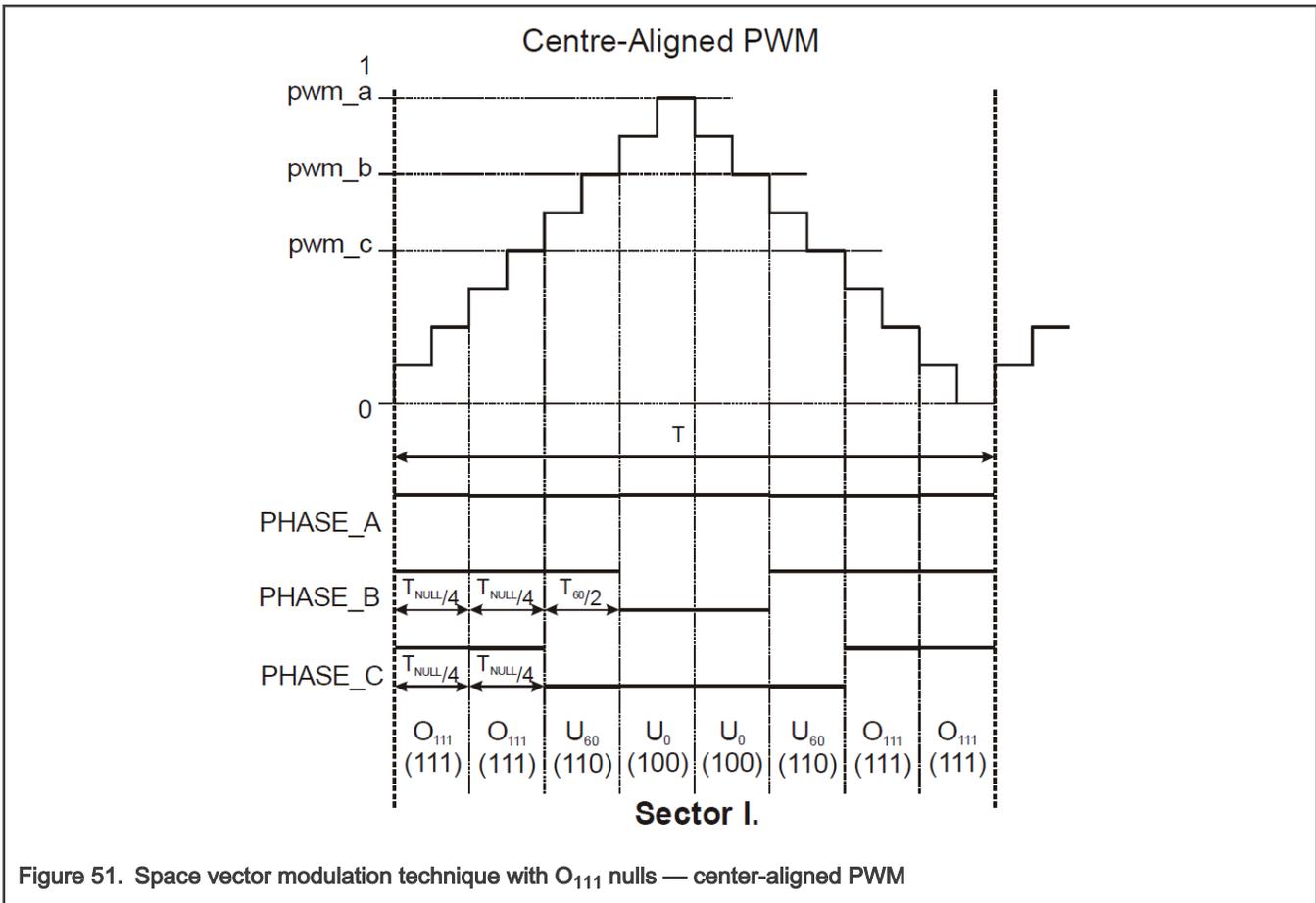


Figure 51. Space vector modulation technique with O₁₁₁ nulls — center-aligned PWM

Figure [GMCLIB_SvmU7n_Img1](#) shows calculated waveforms of the duty-cycle ratios using Space Vector Modulation with O₁₁₁ nulls.

For an accurate calculation of the duty-cycle ratios, direct-α, and quadrature-β components of the stator reference voltage vector, it must be considered that the duty cycle cannot be higher than one (100 %); in other words, the assumption

$$\sqrt{\alpha^2 + \beta^2} \leq 1$$

must be met.

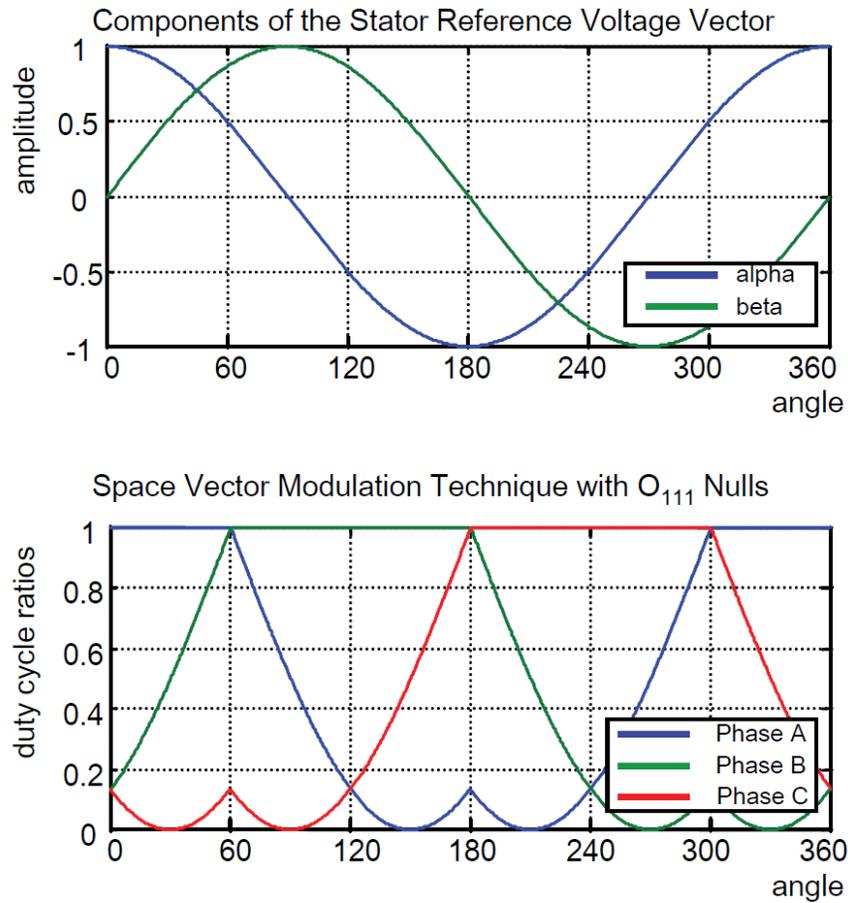


Figure 52. Space vector modulation technique with O_{111} nulls

2.13.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range $<0 ; 1>$. The result may saturate.

The available versions of the [GMCLIB_SvmU7n](#) function are shown in the following table:

Table 19. Function versions

Function name	Input type	Output type	Result type
GMCLIB_SvmU7n_F16	GMCLIB_2COOR_ALBE_T_F16 *	GMCLIB_3COOR_T_F16 *	uint16_t
	General sinusoidal space vector modulation with a 16-bit fractional stationary (α - β) input and a 16-bit fractional three-phase output. The result type is a 16-bit unsigned integer, which indicates the actual SVM sector. The input is within the range $<-1 ; 1>$; the output duty cycle is within the range $<0 ; 1>$. The output sector is an integer value within the range $<1 ; 6>$.		

2.13.2 Declaration

The available [GMCLIB_SvmU7n](#) functions have the following declarations:

```
uint16_t GMCLIB_SvmU7n_F16(const GMCLIB_2COOR_ALBE_T_F16 *psIn, GMCLIB_3COOR_T_F16 *psOut)
```

2.13.3 Function use

The use of the [GMCLIB_SvmU7n](#) function is shown in the following example:

```
#include "gmclib.h"

static uint16_t u16Sector;
static GMCLIB_2COORD_ALBE_T_F16 sAlphaBeta;
static GMCLIB_3COORD_T_F16 sAbc;

void Isr(void);

void main(void)
{
    /* Alpha, Beta structure initialization */
    sAlphaBeta.f16Alpha = FRAC16(0.0);
    sAlphaBeta.f16Beta = FRAC16(0.0);
}

/* Periodical function or interrupt */
void Isr(void)
{
    /* SVM calculation */
    u16Sector = GMCLIB_SvmU7n_F16(&sAlphaBeta, &sAbc);
}
```

2.14 GMCLIB_SvmDpwm

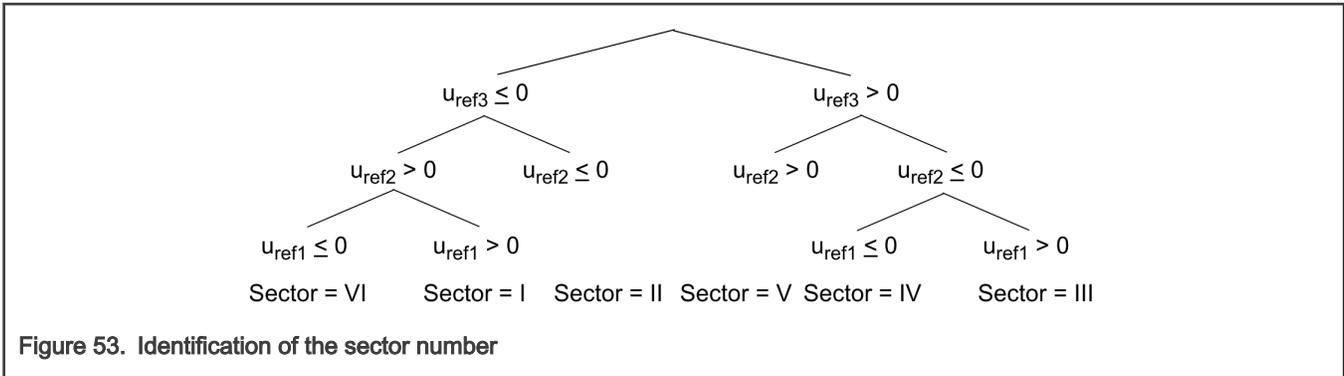
The [GMCLIB_SvmDpwm](#) function calculates the appropriate duty-cycle ratios needed for the generation of the given stator-reference voltage vector using the general non-sinusoidal modulation technique. The [GMCLIB_SvmDpwm](#) function is a subset of the [GMCLIB_SvmExDpwm](#) function and includes a power factor angle input. Both functions are identical if $\varphi = 0$.

The [GMCLIB_SvmDpwm](#) function belongs to the discontinuous PWM modulation techniques for 3-phase voltage inverters. The advantages of the discontinuous PWM technique are lower switching losses, but, on the other hand, it can cause higher harmonic distortion at low modulation indexes. The current sensing at low modulation indexes is more complicated and less precise when compared with the symmetrical modulation techniques like [GMCLIB_SvmStd](#). Therefore, the discontinuous and continuous SVM are usually combined together.

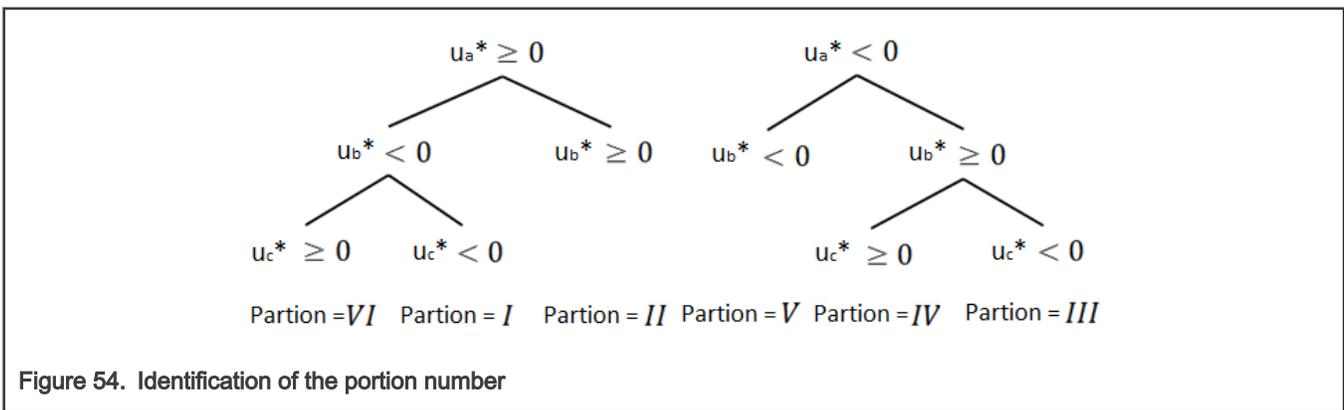
Finding the sector in which the reference stator voltage vector U_S resides is similar to [GMCLIB_SvmStd](#). This is achieved by converting the direct- α and quadrature- β components of the reference stator voltage vector U_S into the balanced 3-phase quantities u_{ref1} , u_{ref2} , and u_{ref3} using the modified Inverse Clarke transformation:

$$\begin{aligned} u_{ref1} &= u_\beta \\ u_{ref2} &= \frac{\sqrt{3}u_\alpha - u_\beta}{2} \\ u_{ref3} &= \frac{-\sqrt{3}u_\alpha - u_\beta}{2} \end{aligned}$$

The sector calculation is based on comparing the 3-phase reference voltages u_{ref1} , u_{ref2} , and u_{ref3} with zero. This computation is described by the following figure:



The knowledge of the sector is necessary for the current sensing especially when shunt resistors are used. The [GMCLIB_SvmDpwm](#) function does not require the sector directly, but it requires the portion identification explained in the following. The Inverse Clarke transformation converts the u_α , u_β voltage components of the reference stator voltage vector U_S to 3-phase voltage components u_a , u_b , and u_c . The portion identification selects the portion from the u_a , u_b , and u_c voltages, based on the following conditions.



Finally, the corresponding duty cycle is selected according to the portion from the column of the following table.

Table 20. Duty cycle calculation from portions

Portions	I	II	III	IV	V	VI
Voltage boundaries	U_{330}, U_{30}	U_{30}, U_{90}	U_{90}, U_{150}	U_{150}, U_{210}	U_{210}, U_{270}	U_{270}, U_{330}
pwm_a	1	$0 - u_{ref3}$	$1 + u_{ref2}$	0	$1 - u_{ref3}$	$0 + u_{ref2}$
pwm_b	$1 - u_{ref2}$	$0 + u_{ref1} = u_\beta$	1	$0 - u_{ref2}$	$1 + u_{ref1} = 1 + u_\beta$	0
pwm_c	$1 + u_{ref3}$	0	$1 - u_{ref1} = 1 - u_\beta$	$0 + u_{ref3}$	1	$0 - u_{ref1} = 0 - u_\beta$

2.14.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range $<0 ; 1$). The result may saturate.

The available versions of the [GMCLIB_SvmDpwm](#) function are shown in the following table:

Table 21. Function versions

Function name	Input type	Output type	Result type
GMCLIB_SvmDpwm_F16	GMCLIB_2COOR_ALBE_T_F16 *	GMCLIB_3COOR_T_F16 *	uint16_t
	Standard discontinuous PWM with a 16-bit fractional stationary (α - β) input, and a 16-bit fractional 3-phase output. The result type is a 16-bit unsigned integer, which indicates the actual SVM sector. The input is within the range $\langle -1 ; 1 \rangle$; the output duty cycle is within the range $\langle 0 ; 1 \rangle$. The output sector is an integer value within the range $\langle 1 ; 6 \rangle$.		

2.14.2 Declaration

The available [GMCLIB_SvmDpwm](#) functions have the following declarations:

```
uint16_t GMCLIB_SvmDpwm_F16(const GMCLIB_2COOR_ALBE_T_F16 *psIn, GMCLIB_3COOR_T_F16 *psOut)
```

2.14.3 Function use

The use of the [GMCLIB_SvmDpwm](#) function is shown in the following example:

```
#include "gmclib.h"

static uint16_t ul6Sector;
static GMCLIB_2COOR_ALBE_T_F16 sAlphaBeta;
static GMCLIB_3COOR_T_F16 sAbc;

void Isr(void);

void main(void)
{
    /* Alpha, Beta structure initialization */
    sAlphaBeta.f16Alpha = FRAC16(0.0);
    sAlphaBeta.f16Beta = FRAC16(0.0);

    /* Periodical function or interrupt */
}

void Isr(void)
{
    /* Standard Discontinuous PWM SVM calculation */
    ul6Sector = GMCLIB_SvmGenDpwm_F16(&sAlphaBeta, &sAbc);
}
```

2.15 GMCLIB_SvmExDpwm

The [GMCLIB_SvmExDpwm](#) function calculates the appropriate duty-cycle ratios needed for the generation of the given stator-reference voltage vector using the general non-sinusoidal modulation technique. The [GMCLIB_SvmExDpwm](#) function is a superset of the [GMCLIB_SvmDpwm](#) function without the power factor angle input.

The [GMCLIB_SvmExDpwm](#) function belongs to the discontinuous PWM modulation techniques for a 3-phase voltage inverter. The advantages of the discontinuous PWM technique are lower switching losses, but, on the other hand, it can cause higher harmonic distortion at low modulation indexes. The current sensing at low modulation indexes is more complicated and less precise when compared to the symmetrical modulation techniques like [GMCLIB_SvmStd](#). Therefore, the discontinuous and continuous SVM are usually combined together.

Finding the sector in which the reference stator voltage vector U_S resides is similar to [GMCLIB_SvmStd](#). This is achieved by converting the direct- α and quadrature- β components of the reference stator voltage vector U_S into the balanced 3-phase quantities u_{ref1} , u_{ref2} , and u_{ref3} using the modified Inverse Clarke transformation:

$$\begin{aligned}
 u_{ref1} &= u_\beta \\
 u_{ref2} &= \frac{\sqrt{3}u_\alpha - u_\beta}{2} \\
 u_{ref3} &= \frac{-\sqrt{3}u_\alpha - u_\beta}{2}
 \end{aligned}$$

The sector calculation is based on comparing the 3-phase reference voltages u_{ref1} , u_{ref2} , and u_{ref3} with zero. This computation is described by the following figure:

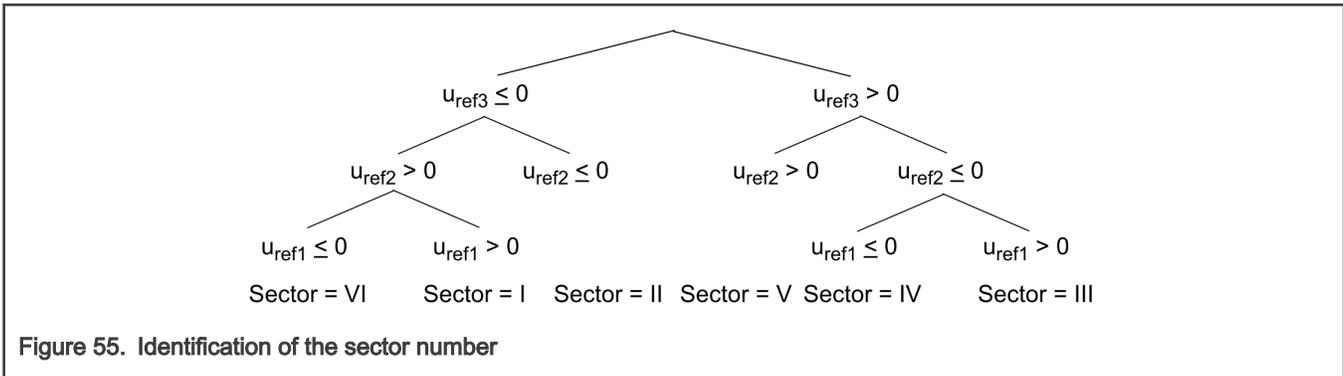


Figure 55. Identification of the sector number

The knowledge of the sector is necessary for the current sensing especially when shunt resistors are used. The [GMCLIB_SvmExDpwm](#) function does not require the sector directly, but it requires the portion identification explained in following text. The Park transformation uses the phase shift of the generated phase voltages and currents - φ angle to rotate the reference stator voltage vector U_S to U_S^* with the u_α^* , u_β^* components. The inverse Clarke transformation converts the u_α^* , u_β^* voltage components to 3-phase voltage components u_a^* , u_b^* , and u_c^* . The portion identification selects the portion from the u_a^* , u_b^* , and u_c^* voltages based on the following conditions.

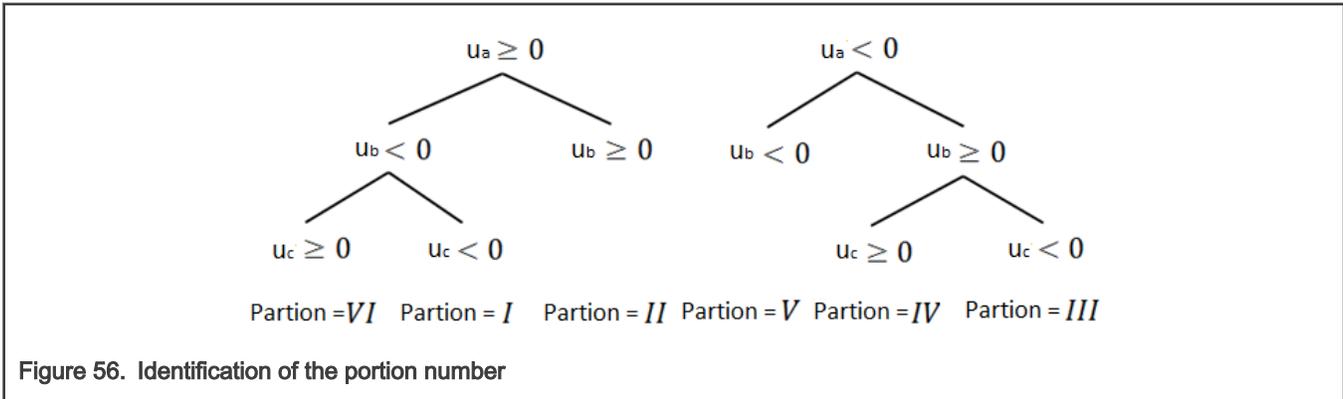


Figure 56. Identification of the portion number

Finally, the corresponding duty cycle is selected according to the portion from the column of the following table.

Table 22. Duty cycle calculation from portions

Portions	I	II	III	IV	V	VI
Voltage boundaries	U_{330}, U_{30}	U_{30}, U_{90}	U_{90}, U_{150}	U_{150}, U_{210}	U_{210}, U_{270}	U_{270}, U_{330}
pwm_a	1	$0 - u_{ref3}$	$1 + u_{ref2}$	0	$1 - u_{ref3}$	$0 + u_{ref2}$

Table continues on the next page...

Table 22. Duty cycle calculation from portions (continued)

pwm_b	$1 - u_{ref2}$	$0 + u_{ref1} = u_{\beta}$	1	$0 - u_{ref2}$	$1 + u_{ref1} = 1 + u_{\beta}$	0
pwm_c	$1 + u_{ref3}$	0	$1 - u_{ref1} = 1 - u_{\beta}$	$0 + u_{ref3}$	1	$0 - u_{ref1} = 0 - u_{\beta}$

2.15.1 Available versions

This function is available in the following versions:

- Fractional output - the output is the fractional portion of the result; the result is within the range $<0 ; 1)$. The result may saturate.

The available versions of the [GMCLIB_SvmExDpwm](#) function are shown in the following table:

Table 23. Function versions

Function name	Input type	Output type	Result type
GMCLIB_SvmExDpwm_F16	GMCLIB_2COOR_ALBE_T_F16 *	GMCLIB_3COOR_T_F16 *	uint16_t
	GMCLIB_2COOR_SINCOS_T_F16 *		
Extended discontinuous PWM with a 16-bit fractional stationary (α - β) input, the second input using a 16-bit fractional ($\sin(\varphi) / \cos(\varphi)$) structure of φ angle ($-1/6 ; 1/6$) in fraction corresponding ($-\pi/6 ; \pi/6$) in radians - angle of the power factor, it is a phase shift of the generated phase voltages and currents and a 16-bit fractional 3-phase output. The result type is a 16-bit unsigned integer which indicates the actual SVM sector. The input is within the range $<-1 ; 1)$; the output duty cycle is within the range $<0 ; 1)$. The output sector is an integer value within the range $<1 ; 6>$.			

2.15.2 Declaration

The available [GMCLIB_SvmExDpwm](#) functions have the following declarations:

```
uint16_t GMCLIB_SvmExDpwm_F16(const GMCLIB_2COOR_ALBE_T_F16 *psIn, const GMCLIB_2COOR_SINCOS_T_F16 *psAngle, GMCLIB_3COOR_T_F16 *psOut)
```

2.15.3 Function use

The use of the [GMCLIB_SvmExDpwm](#) function is shown in the following example:

```
#include "gmclib.h"

static uint16_t u16Sector;
static GMCLIB_2COOR_ALBE_T_F16 sAlphaBeta;
static GMCLIB_2COOR_SINCOS_T_F16 sAlphaBeta;
static GMCLIB_3COOR_T_F16 sAbc;

void Isr(void);

void main(void)
{
    /* Alpha, Beta structure initialization */
    sAlphaBeta.f16Alpha = FRAC16(0.0);
    sAlphaBeta.f16Beta = FRAC16(0.0);

    /* Power factor angle structure initialization */
    sAngle.f16Cos = FRAC16(1.0);
    sAngle.f16Sin = FRAC16(0.0);
}
```

```
/* Periodical function or interrupt */  
void Isr(void)  
{  
    /* Extended Discontinues PWM calculation */  
    u16Sector = GMCLIB_SvmExDpwm_F16(&sAlphaBeta, &sAngle, &sAbc);  
}
```

Appendix A

Library types

A.1 bool_t

The `bool_t` type is a logical 16-bit type. It is able to store the boolean variables with two states: TRUE (1) or FALSE (0). Its definition is as follows:

```
typedef unsigned short bool_t;
```

The following figure shows the way in which the data is stored by this type:

Table 24. Data storage

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Value	Unused															Logical	
TRUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	0				0				0				1				
FALSE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0				0				0				0				

To store a logical value as `bool_t`, use the `FALSE` or `TRUE` macros.

A.2 uint8_t

The `uint8_t` type is an unsigned 8-bit integer type. It is able to store the variables within the range <0 ; 255>. Its definition is as follows:

```
typedef unsigned char uint8_t;
```

The following figure shows the way in which the data is stored by this type:

Table 25. Data storage

	7	6	5	4	3	2	1	0
Value	Integer							
255	1	1	1	1	1	1	1	1
	F				F			

Table continues on the next page...

Table 25. Data storage (continued)

11	0	0	0	0	1	0	1	1
	0				B			
124	0	1	1	1	1	1	0	0
	7				C			
159	1	0	0	1	1	1	1	1
	9				F			

A.3 uint16_t

The `uint16_t` type is an unsigned 16-bit integer type. It is able to store the variables within the range $\langle 0 ; 65535 \rangle$. Its definition is as follows:

```
typedef unsigned short uint16_t;
```

The following figure shows the way in which the data is stored by this type:

Table 26. Data storage

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	Integer															
65535	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	F				F				F				F			
5	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
	0				0				0				5			
15518	0	0	1	1	1	1	0	0	1	0	0	1	1	1	1	0
	3				C				9				E			
40768	1	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0
	9				F				4				0			

A.4 uint32_t

The `uint32_t` type is an unsigned 32-bit integer type. It is able to store the variables within the range $\langle 0 ; 4294967295 \rangle$. Its definition is as follows:

```
typedef unsigned long uint32_t;
```

The following figure shows the way in which the data is stored by this type:

Table 27. Data storage

	31		24 23		16 15		8 7		0
Value	Integer								
4294967295	F	F	F	F	F	F	F	F	F
2147483648	8	0	0	0	0	0	0	0	0
55977296	0	3	5	6	2	5	5	0	
3451051828	C	D	B	2	D	F	3	4	

A.5 int8_t

The `int8_t` type is a signed 8-bit integer type. It is able to store the variables within the range $\langle -128 ; 127 \rangle$. Its definition is as follows:

```
typedef char int8_t;
```

The following figure shows the way in which the data is stored by this type:

Table 28. Data storage

	7	6	5	4	3	2	1	0
Value	Sign	Integer						
127	0	1	1	1	1	1	1	1
	7				F			
-128	1	0	0	0	0	0	0	0
	8				0			
60	0	0	1	1	1	1	0	0
	3				C			

Table continues on the next page...

Table 28. Data storage (continued)

-97	1	0	0	1	1	1	1	1
	9				F			

A.6 int16_t

The `int16_t` type is a signed 16-bit integer type. It is able to store the variables within the range $\langle -32768 ; 32767 \rangle$. Its definition is as follows:

```
typedef short int16_t;
```

The following figure shows the way in which the data is stored by this type:

Table 29. Data storage

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	Sign	Integer														
32767	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	7			F				F				F				
-32768	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8			0				0				0				
15518	0	0	1	1	1	1	0	0	1	0	0	1	1	1	1	0
	3			C				9				E				
-24768	1	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0
	9			F				4				0				

A.7 int32_t

The `int32_t` type is a signed 32-bit integer type. It is able to store the variables within the range $\langle -2147483648 ; 2147483647 \rangle$. Its definition is as follows:

```
typedef long int32_t;
```

The following figure shows the way in which the data is stored by this type:

Table 30. Data storage

<i>Table continues on the next page...</i>
--

Table 30. Data storage (continued)

Value	31	24 23		16 15		8 7		0
	S	Integer						
2147483647	7	F	F	F	F	F	F	F
-2147483648	8	0	0	0	0	0	0	0
55977296	0	3	5	6	2	5	5	0
-843915468	C	D	B	2	D	F	3	4

A.8 frac8_t

The `frac8_t` type is a signed 8-bit fractional type. It is able to store the variables within the range $<-1 ; 1$). Its definition is as follows:

```
typedef char frac8_t;
```

The following figure shows the way in which the data is stored by this type:

Table 31. Data storage

Value	7	6	5	4	3	2	1	0
	Sign	Fractional						
0.99219	0	1	1	1	1	1	1	1
-1.0	7				F			
	1	0	0	0	0	0	0	0
0.46875	8				0			
	0	0	1	1	1	1	0	0
-0.75781	3				C			
	1	0	0	1	1	1	1	1
	9				F			

To store a real number as `frac8_t`, use the `FRAC8` macro.

Table 33. Data storage (continued)

-1.0	8	0	0	0	0	0	0	0	0
0.02606645970	0	3	5	6	2	5	5	0	
-0.3929787632	C	D	B	2	D	F	3	4	

To store a real number as `frac32_t`, use the `FRAC32` macro.

A.11 `acc16_t`

The `acc16_t` type is a signed 16-bit fractional type. It is able to store the variables within the range $<-256 ; 256$). Its definition is as follows:

```
typedef short acc16_t;
```

The following figure shows the way in which the data is stored by this type:

Table 34. Data storage

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	Sign	Integer							Fractional							
255.9921875	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	7			F				F			F					
-256.0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8			0				0			0					
1.0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	0			0				8			0					
-1.0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	F			F				8			0					
13.7890625	0	0	0	0	0	1	1	0	1	1	1	0	0	1	0	1
	0			6				E			5					
-89.71875	1	1	0	1	0	0	1	1	0	0	1	0	0	1	0	0
	D			3				2			4					

To store a real number as `acc16_t`, use the `ACC16` macro.

A.12 `acc32_t`

The `acc32_t` type is a signed 32-bit accumulator type. It is able to store the variables within the range $<-65536 ; 65536$). Its definition is as follows:

```
typedef long acc32_t;
```

The following figure shows the way in which the data is stored by this type:

Table 35. Data storage

Value	31	24 23			16 15		8 7		0
	S	Integer				Fractional			
65535.999969	7	F	F	F	F	F	F	F	
-65536.0	8	0	0	0	0	0	0	0	
1.0	0	0	0	0	8	0	0	0	
-1.0	F	F	F	F	8	0	0	0	
23.789734	0	0	0	B	E	5	1	6	
-1171.306793	F	D	B	6	5	8	B	C	

To store a real number as `acc32_t`, use the `ACC32` macro.

A.13 `float_t`

The `float_t` type is a signed 32-bit single precision floating-point type, defined by IEEE 754. It is able to store the full precision (normalized) finite variables within the range $<-3.40282 \cdot 10^{38} ; 3.40282 \cdot 10^{38}$) with the minimum resolution of 2^{-23} . The smallest normalized number is $\pm 1.17549 \cdot 10^{-38}$. Nevertheless, the denormalized numbers (with reduced precision) reach yet lower values, from $\pm 1.40130 \cdot 10^{-45}$ to $\pm 1.17549 \cdot 10^{-38}$. The standard also defines the additional values:

- Negative zero
- Infinity
- Negative infinity
- Not a number

The 32-bit type is composed of:

- Sign (bit 31)
- Exponent (bits 23 to 30)
- Mantissa (bits 0 to 22)

The conversion of the number is straightforward. The sign of the number is stored in bit 31. The binary exponent is decoded as an integer from bits 23 to 30 by subtracting 127. The mantissa (fraction) is stored in bits 0 to 22. An invisible leading bit (it is not


```
float_t fltC;
} GMCLIB_3COOR_T_FLT;
```

The structure description is as follows:

Table 40. GMCLIB_3COOR_T_FLT members description

Type	Name	Description
float_t	fltA	A component; 32-bit single precision floating-point type
float_t	fltB	B component; 32-bit single precision floating-point type
float_t	fltC	C component; 32-bit single precision floating-point type

A.16 GMCLIB_2COOR_AB_T_F16

The [GMCLIB_2COOR_AB_T_F16](#) structure type corresponds to the general two-phase stationary coordinate system, based on the A and B orthogonal components. Each member is of the [frac16_t](#) data type. The structure definition is as follows:

```
typedef struct
{
    frac16_t f16A;
    frac16_t f16B;
} GMCLIB_2COOR_AB_T_F16;
```

The structure description is as follows:

Table 41. GMCLIB_2COOR_AB_T_F16 members description

Type	Name	Description
frac16_t	f16A	A-component; 16-bit fractional type
frac16_t	f16B	B-component; 16-bit fractional type

A.17 GMCLIB_2COOR_AB_T_F32

The [GMCLIB_2COOR_AB_T_F32](#) structure type corresponds to the general two-phase stationary coordinate system, based on the A and B orthogonal components. Each member is of the [frac32_t](#) data type. The structure definition is as follows:

```
typedef struc
{
    frac32_t f32Alpha;
    frac32_t f32Beta;
} GMCLIB_2COOR_AB_T_F32;
```

The structure description is as follows:

Table 42. GMCLIB_2COOR_AB_T_F32 members description

Type	Name	Description
frac32_t	f32A	A component; 32-bit fractional type
frac32_t	f32B	B component; 32-bit fractional type

A.18 GMCLIB_2COOR_ALBE_T_F16

The [GMCLIB_2COOR_ALBE_T_F16](#) structure type corresponds to the two-phase stationary coordinate system, based on the Alpha and Beta orthogonal components. Each member is of the [frac16_t](#) data type. The structure definition is as follows:

```
typedef struct
{
    frac16_t f16Alpha;
    frac16_t f16Beta;
} GMCLIB_2COOR_ALBE_T_F16;
```

The structure description is as follows:

Table 43. GMCLIB_2COOR_ALBE_T_F16 members description

Type	Name	Description
frac16_t	f16Apha	α -component; 16-bit fractional type
frac16_t	f16Beta	β -component; 16-bit fractional type

A.19 GMCLIB_2COOR_ALBE_T_FLT

The [GMCLIB_2COOR_ALBE_T_FLT](#) structure type corresponds to the two-phase stationary coordinate system based on the Alpha and Beta orthogonal components. Each member is of the [float_t](#) data type. The structure definition is as follows:

```
typedef struct
{
    float_t fltAlpha;
    float_t fltBeta;
} GMCLIB_2COOR_ALBE_T_FLT;
```

The structure description is as follows:

Table 44. GMCLIB_2COOR_ALBE_T_FLT members description

Type	Name	Description
float_t	fltApha	α -component; 32-bit single precision floating-point type
float_t	fltBeta	β -component; 32-bit single precision floating-point type

A.20 GMCLIB_2COOR_DQ_T_F16

The [GMCLIB_2COOR_DQ_T_F16](#) structure type corresponds to the two-phase rotating coordinate system, based on the D and Q orthogonal components. Each member is of the [frac16_t](#) data type. The structure definition is as follows:

```
typedef struct
{
    frac16_t f16D;
    frac16_t f16Q;
} GMCLIB_2COOR_DQ_T_F16;
```

The structure description is as follows:

Table 45. GMCLIB_2COOR_DQ_T_F16 members description

Type	Name	Description
frac16_t	f16D	D-component; 16-bit fractional type
frac16_t	f16Q	Q-component; 16-bit fractional type

A.21 GMCLIB_2COOR_DQ_T_F32

The [GMCLIB_2COOR_DQ_T_F32](#) structure type corresponds to the two-phase rotating coordinate system, based on the D and Q orthogonal components. Each member is of the [frac32_t](#) data type. The structure definition is as follows:

```
typedef struct
{
    frac32_t f32D;
    frac32_t f32Q;
} GMCLIB_2COOR_DQ_T_F32;
```

The structure description is as follows:

Table 46. GMCLIB_2COOR_DQ_T_F32 members description

Type	Name	Description
frac32_t	f32D	D-component; 32-bit fractional type
frac32_t	f32Q	Q-component; 32-bit fractional type

A.22 GMCLIB_2COOR_DQ_T_FLT

The [GMCLIB_2COOR_DQ_T_FLT](#) structure type corresponds to the two-phase rotating coordinate system, based on the D and Q orthogonal components. Each member is of the [float_t](#) data type. The structure definition is as follows:

```
typedef struct
{
    float_t fltD;
    float_t fltQ;
} GMCLIB_2COOR_DQ_T_FLT;
```

The structure description is as follows:

Table 47. GMCLIB_2COOR_DQ_T_FLT members description

Type	Name	Description
float_t	fltD	D-component; 32-bit single precision floating-point type
float_t	fltQ	Q-component; 32-bit single precision floating-point type

A.23 GMCLIB_2COOR_SINCOS_T_F16

The [GMCLIB_2COOR_SINCOS_T_F16](#) structure type corresponds to the two-phase coordinate system, based on the Sin and Cos components of a certain angle. Each member is of the [frac16_t](#) data type. The structure definition is as follows:

```
typedef struct
{
    frac16_t f16Sin;
```

```

frac16_t f16Cos;
} GMCLIB_2COOR_SINCOS_T_F16;

```

The structure description is as follows:

Table 48. GMCLIB_2COOR_SINCOS_T_F16 members description

Type	Name	Description
frac16_t	f16Sin	Sin component; 16-bit fractional type
frac16_t	f16Cos	Cos component; 16-bit fractional type

A.24 GMCLIB_2COOR_SINCOS_T_FLT

The `GMCLIB_2COOR_SINCOS_T_FLT` structure type corresponds to the two-phase coordinate system, based on the Sin and Cos components of a certain angle. Each member is of the `float_t` data type. The structure definition is as follows:

```

typedef struct
{
    float_t fltSin;
    float_t fltCos;
} GMCLIB_2COOR_SINCOS_T_FLT;

```

The structure description is as follows:

Table 49. GMCLIB_2COOR_SINCOS_T_FLT members description

Type	Name	Description
float_t	fltSin	Sin component; 32-bit single precision floating-point type
float_t	fltCos	Cos component; 32-bit single precision floating-point type

A.25 FALSE

The `FALSE` macro serves to write a correct value standing for the logical FALSE value of the `bool_t` type. Its definition is as follows:

```

#define FALSE ((bool_t)0)

```

```

#include "mlib.h"

static bool_t bVal;

void main(void)
{
    bVal = FALSE;          /* bVal = FALSE */
}

```

A.26 TRUE

The **TRUE** macro serves to write a correct value standing for the logical TRUE value of the `bool_t` type. Its definition is as follows:

```
#define TRUE ((bool_t)1)
```

```
#include "mlib.h"

static bool_t bVal;

void main(void)
{
    bVal = TRUE;           /* bVal = TRUE */
}
```

A.27 FRAC8

The **FRAC8** macro serves to convert a real number to the `frac8_t` type. Its definition is as follows:

```
#define FRAC8(x) ((frac8_t)((x) < 0.9921875 ? ((x) >= -1 ? (x)*0x80 : 0x80) : 0x7F))
```

The input is multiplied by 128 ($=2^7$). The output is limited to the range `<0x80 ; 0x7F>`, which corresponds to `<-1.0 ; 1.0-2-7>`.

```
#include "mlib.h"

static frac8_t f8Val;

void main(void)
{
    f8Val = FRAC8(0.187);           /* f8Val = 0.187 */
}
```

A.28 FRAC16

The **FRAC16** macro serves to convert a real number to the `frac16_t` type. Its definition is as follows:

```
#define FRAC16(x) ((frac16_t)((x) < 0.999969482421875 ? ((x) >= -1 ? (x)*0x8000 : 0x8000) : 0x7FFF))
```

The input is multiplied by 32768 ($=2^{15}$). The output is limited to the range `<0x8000 ; 0x7FFF>`, which corresponds to `<-1.0 ; 1.0-2-15>`.

```
#include "mlib.h"

static frac16_t f16Val;

void main(void)
{
    f16Val = FRAC16(0.736);           /* f16Val = 0.736 */
}
```

A.29 FRAC32

The **FRAC32** macro serves to convert a real number to the **frac32_t** type. Its definition is as follows:

```
#define FRAC32(x) ((frac32_t)((x) < 1 ? ((x) >= -1 ? (x)*0x80000000 : 0x80000000) : 0x7FFFFFFF))
```

The input is multiplied by 2147483648 ($=2^{31}$). The output is limited to the range $\langle 0x80000000 ; 0x7FFFFFFF \rangle$, which corresponds to $\langle -1.0 ; 1.0 \cdot 2^{-31} \rangle$.

```
#include "mlib.h"

static frac32_t f32Val;

void main(void)
{
    f32Val = FRAC32(-0.1735667);          /* f32Val = -0.1735667 */
}
```

A.30 ACC16

The **ACC16** macro serves to convert a real number to the **acc16_t** type. Its definition is as follows:

```
#define ACC16(x) ((acc16_t)((x) < 255.9921875 ? ((x) >= -256 ? (x)*0x80 : 0x8000) : 0x7FFF))
```

The input is multiplied by 128 ($=2^7$). The output is limited to the range $\langle 0x8000 ; 0x7FFF \rangle$ that corresponds to $\langle -256.0 ; 255.9921875 \rangle$.

```
#include "mlib.h"

static acc16_t a16Val;

void main(void)
{
    a16Val = ACC16(19.45627);          /* a16Val = 19.45627 */
}
```

A.31 ACC32

The **ACC32** macro serves to convert a real number to the **acc32_t** type. Its definition is as follows:

```
#define ACC32(x) ((acc32_t)((x) < 65535.999969482421875 ? ((x) >= -65536 ? (x)*0x8000 : 0x80000000) : 0x7FFFFFFF))
```

The input is multiplied by 32768 ($=2^{15}$). The output is limited to the range $\langle 0x80000000 ; 0x7FFFFFFF \rangle$, which corresponds to $\langle -65536.0 ; 65536.0 \cdot 2^{-15} \rangle$.

```
#include "mlib.h"

static acc32_t a32Val;

void main(void)
```

```
{  
  a32Val = ACC32(-13.654437);          /* a32Val = -13.654437 */  
}
```

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Limited warranty and liability— Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

Right to make changes - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Security— Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, ICODE, JCOP, LIFE, VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, Altivec, CodeWarrior, ColdFire, ColdFire+, the Energy Efficient Solutions logo, Kinetic, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, Tower, TurboLink, EdgeScale, EdgeLock, eIQ, and Immersive3D are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, µVision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. M, M Mobileye and other Mobileye trademarks or logos appearing herein are trademarks of Mobileye Vision Technologies Ltd. in the United States, the EU and/or other jurisdictions.

© NXP B.V. 2021.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 01 November 2021
Document identifier: CM0GMCLIBUG